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FEATURES:

- VERY LOW PHASE NOISE
- EXCELLENT STABILITY
- COAXIAL RESONATOR OSCILLATOR
- OPTIMIZED BANDWIDTHS
- LOOP NOISE INDEPENDENT OF STEP SIZE
- FAST SWITCHING (<10 µsec)

DESCRIPTION:

Synergy's FN3000 series of Fractional-N Synthesizers consist of a transistor oscillator with a High Q ceramic resonator at the base. This very low noise voltage controlled oscillator is synchronized using Synergy's ultra low noise fractional N Custom PLL chip with a noise floor of less than -160 dBm. The advanced Fractional Division N implementation with digital compensation allows step sizes from 1 KHz to 1 MHz and exceptionally low phase noise. Switching speed is <10 µsec.

SPECIFICATIONS:

Available Frequency :	**100 - 3000 MHz***
Bandwidth:	**20 MHz to 300 MHz◆**
Step Size:	**1 KHz to 1 MHz**
Reference Input Frequency:	**120 MHz (Typical)**
Reference Input:	**+8 dBm to +10 dBm**
Bias Voltage:	**Vcc_1 = 5 VDC @ <200 mA**
	Vcc_2 = 5 VDC @ <300 mA
	Vcc_3 = 5 VDC @ <150 mA
	Vcc_4 = 9 to 18 VDC @ <50 mA**
Output Power:	**+5 dBm ±2 dB**
Output Impedance:	**50 Ω (Nom)**
Harmonic Suppression:	**15 dBc (Min)**
VSWR:	**1.8:1 (Nom)**
Typical Phase Noise : (120 MHz Reference)	**-100 dBc/Hz @ 100 Hz offset**
	-100 dBc/Hz @ 1K Hz offset
	-112 dBc/Hz @ 10 KHz offset
	-130 dBc/Hz @ 100 KHz offset
	-150 dBc/Hz @ 1 MHz offset
Programming:	**Serial**
Operating Temperature Range:	**-30° to +70°C**

Note:

***** For frequencies above 1200 MHz, subharmonic level is -30 dBc (Min.)

****** Depends on bandwidth

◆ For more information contact factory.

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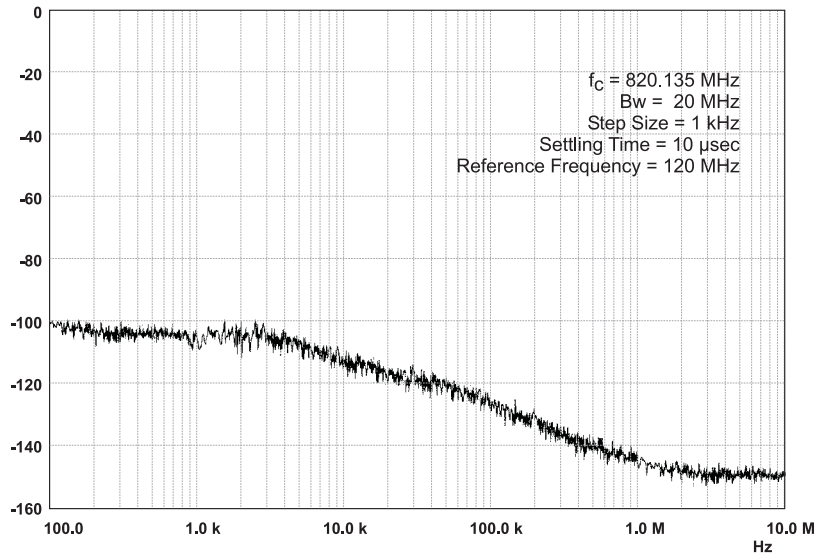
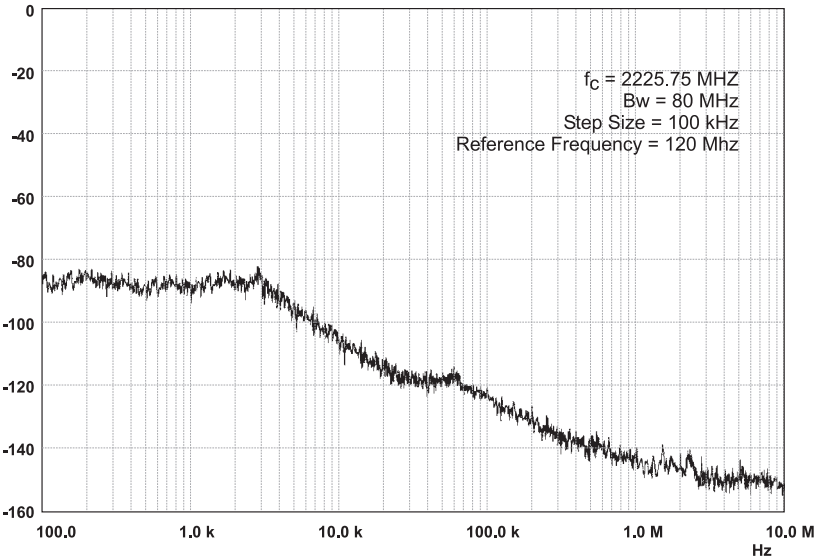
PHASE NOISE PLOTS

- 500 to 1200 MHz
- Narrow bandwidth (10 - 40 MHz)
- Ceramic resonator based high-Q oscillator
- High fractionality leading to better stability & lower step size
- Excellent phase noise performance
- Spurious suppression better than 70 dB
- Fast switching speed (10 µsec on select models)



- 1200 to 3000 MHz
- Wide bandwidth (50 to 300 MHz)
- Ceramic resonator based high-Q oscillator
- Sub-harmonic suppression better than 30 dB
- Step size from 1 kHz to 1 MHz
- (optional) Wider loop bandwidth for improved microphonic effects



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Synergy introduces a new series of fractional-*N* synthesizers that offer high resolution, fast switching and low phase noise compared to conventional PLL-based synthesizers. They combine the best of analog and digital technologies to provide this enhanced performance. Synergy's fractional-*N* synthesizers are most ideal for improved signal-to-noise ratio (SNR) and spurious-free dynamic range for cellular, PCS and similar base-station systems. They offer smaller step size (<25 kHz, smaller than the reference frequency). A variety of models are available in the frequency range from 500 to 3000 MHz, in surface-mount packages and connectorized versions, to meet the varying needs of the industry.

What is Fractional-N Synthesis?

In a conventional PLL synthesizer, the divisor *N*, by which the output frequency is divided for comparison with the reference frequency, must be an integer. Such a PLL has a channel resolution equal to the reference (typically 25 to 1000 kHz). In a fractional-*N* synthesizer, the output frequency f_o is given by

$$f_o = (N + 1/M)f_r$$

where f_r is the reference frequency at the phase detector (typically 5 to 50 MHz) and *N* and *M* are integers. From this equation, we produce the effect of dividing f_o by a non-integer, allowing step sizes smaller than the reference. Fractionality is achieved by dividing the output frequency by *N* + 1 every *M* cycles and dividing by *N* the rest of the time. The synthesizer toggles between the above two frequencies, the average of which over a very small time interval (such as 1 ms) is the desired output frequency. This process creates discrete spurious outputs. A digital compensation circuit "averages" these disturbances into a clean, single-frequency output, cancelling unwanted output frequencies (referred to as *spurs*).

Synergy's fractional-*N* synthesizer is at least 10 times faster than a conventional synthesizer, with close-in (10 to 1000 Hz from the carrier) phase noise performance that is typically 20 to 40 dB better.

SPECIAL FEATURES

✓ Controllable via an RS-232 serial bus or with an optional 6-bit parallel bus for applications requiring microsecond switching speeds.

✓ Low spurious output is guaranteed by on-board, low-noise voltage regulators and high-quality decoupling networks, Intelligent choice of reference to avoid beat notes, and proper selection of sigma-delta converter noise breakpoint versus reference noise in addition to the fractional-*N* principle itself.

✓ For very low phase noise applications, an internal high-voltage dc supply (28 V) allows the use of VCOs with low tuning sensitivity and improved phase noise performance.

✓ Can be driven with references from 80 to 130 MHz (model dependent).

The close-in phase noise depends on the output frequency and the reference. The fractional-*N* synthesizer also exhibits enhanced microphonic performance due to the wider loop bandwidths used. Wide-ranging loop bandwidths (typically 10 to 100 kHz) are possible and can be chosen by the user.

The basic building blocks of a high-quality fractional-*N* synthesizer are: a VCO with low phase noise, frequency dividers, a dual-modulus divider, a phase detector, a sigma-delta modulator, an active LPF, and a buffer amplifier (optional), besides a high-quality, external reference-frequency source. Fig. 1 shows the functional block diagram of Synergy's fractional-*N* synthesizer.

Improved Phase-Noise Performance

In general, different portions of a PLL synthesizer determine its close-in and far-from-carrier phase-noise performance as follows:

- *At offsets within the loop bandwidth*, the phase noise is determined by the loop components, such as dividers, the phase detector, other active components, and the external reference source. The resultant noise level at the phase detector is deteriorated at the output by 20 log(*N*).
- *At offsets outside the loop bandwidth*, the phase noise is determined solely by the quality of the VCO.

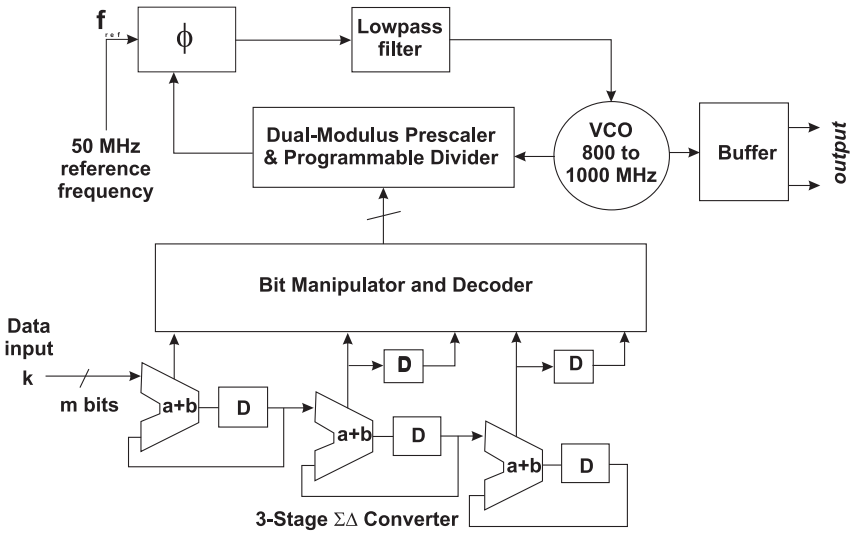

Fig. 1 — Fractional-*N* Synthesizer block diagram

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In conventional PLLs operating at small step sizes, the division ratio is large because the step size must be equal to the reference frequency at the phase detector. As a result, significant phase-noise degradation occurs according to the 20 log(*N*) relationship. At the same time, because the loop bandwidth must be narrow enough to provide sufficient reference suppression, the frequency span over which the loop controls the system's phase-noise performance is restricted. Also, narrower loop bandwidths equate to slower switching speeds.

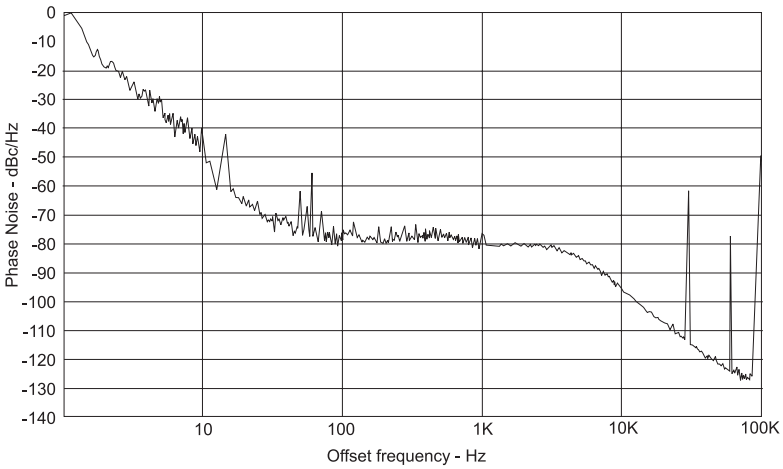

Fig. 2(a) — Phase noise of a conventional synthesizer

In a fractional-*N* synthesizer, the division ratio is much smaller, due to the fact that the comparison is done at a much higher frequency (typically 50 MHz) compared to the step size, thus minimizing the 20 log(*N*) phase-noise degradation at offsets within the loop bandwidth. Because the reference frequency at the phase detector can now be much higher for small step sizes, the loop bandwidth can be much greater, reducing switching time and widening the frequency span over which the loop controls the system's phase-noise performance. This results in the simultaneous achievement of low close-in phase noise and fast switching even with smaller step sizes (<25 kHz). To derive the full benefits of the fractional-*N* synthesizer utilizing a three-stage sigma-delta modulator, it is recommended to use a quiet high-frequency reference source to achieve excellent phase noise performance. Figures 2a and 2b shows the phase-noise plots for conventional fractional-*N* and synthesizers, respectively.

Who Needs Fractional-*N* Synthesizers?

Synthesizers are found in most wireless applications: from battery-operated cellular and cordless telephones to wireless networks, base stations and commercial test equipment. Fractional-*N* synthesizers, based on advanced digital circuitry, offer much higher resolution compared to traditional synthesizers based on multiloop techniques.

Typical wireless applications require steps of:

• 5 kHz • 15 kHz • 25 kHz
• 30 kHz • 50 to 1000 kHz

or arbitrary sizes and offsets. The fractional-*N* technique can be enhanced to provide quasi-arbitrary resolutions of better than *1 millihertz* (mHz). It can replace complicated multiloop synthesizers in any type of receiver, signal generator, or synthesizer-based system.

With an upper frequency limit of about 3 to 3.2 GHz, Synergy's fractional-*N* synthesizers are well-suited for such critical applications as low-noise signal generators. They can compete with a large number of synthesizers on the market, and can also be used as a building block for OEM synthesizer designs.

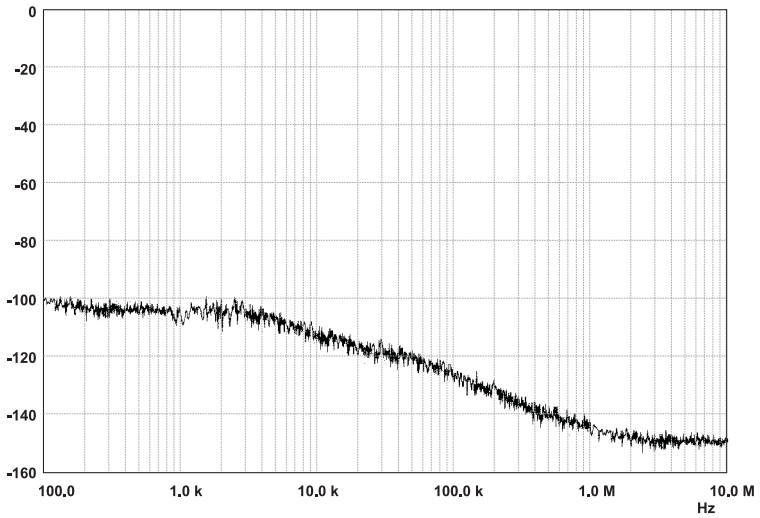

Fig. 2(b) — Phase noise plot of fractional-*N* synthesizer FN3000 810-830 using 120-MHz custom built crystal reference source.

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1. Introduction

Synergy's FN3000-series fractional-*N* synthesizers are programmed with serial data through a three-wire line carrying CLOCK, DATA, and STROBE signals. The programming data sent to the synthesizer resides in sixteen 8-bit registers at four address locations (Figure 1).

D31.....D24	D23.....D16	D15.....D8	D7.....D0	A7.....A0
R33	R32	R31	R30	00000011
R43	R42	R41	R40	00000100
R53	R52	R51	R50	00000101
R93	R92	R91	R90	00001001

2. Frequency Command Format

Command Contents. Setting the synthesizer to a given frequency requires the communication of the binary equivalent of a *fractional-division number* determined by the formula

$$M = \left(\frac{F_{\text{VCO}} \times R}{P \times F_{\text{ref}}} \right) - 1 \qquad (1)$$

where

M = Fractional-division number
R = Reference-frequency division number
P = RF prescaler divisor
F_{VCO} = VCO frequency in MHz
F_{ref} = Reference frequency in MHz

The parameters *R* and *P* are set at the factory for each synthesizer model depending on the VCO frequency and bandwidth, and electrical performance requirements, such as spurious suppression, phase noise, and so on.

The reference division number *R* can be set to one of two factory-defined values, one of which serves as a default. *R* must be changed from its default value for certain frequencies, which are specific to the FN3000 version used, to achieve the best spurious and phase-noise performance. The user is provided with a list of these frequencies and the new *R* value, which must be used to calculate *M* using Equation (1). (Appendix 1 shows a sample list of such frequencies for the example presented in Section 5, below.)

The binary equivalent of the division number *M* is sent to the synthesizer as data bits combined with address and factory-determined command bits. The integer portion of *M* is loaded as a 16-bit binary word into two registers. The decimal portion of *M* is loaded as a 40-bit binary word into two registers.

☞ Synergy provides the user with an executable file for evaluation of the fractional synthesizer. Synergy also provides a program to calculate the binary equivalent of the integer and fractional parts of the division number.

Command Structure. For each frequency, the programming information sent to the synthesizer consists of 160 bits of data sent as four 40-bit packets comprising the division number in binary form, plus control and address bits. Each 40-bit packet consists of 32 bits of data and an 8-bit address, with the most significant bit (MSB) loaded first. Figure 2 shows the data format for one address location.

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D31	D30	D29	...	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0

Shift direction, MSB first.

Figure 2: Data format for one address location.

The 56-bit representation of *M* is mapped across the data loaded into the 04h and 05h address spaces as shown in Figure 3.

A7-A0	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
03h	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	X	Y	Y	Y	Y	Y
	Register 33								Register 32								Register 31								Register 30							
04h																																2^{-40}
	Register 43								Register 42								Register 41								Register 40							
05h	Y	Y	Y	Y	Y	Y	Y	Y									2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}					
	Register 53								Register 52								Register 51								Register 50							
09h	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	Register 93								Register 92								Register 91								Register 90							

X = 0 for all frequencies except as listed on the ***R* & D5 versus Frequency** specification sheet for the FN3000 version supplied.
□ = Bits conveying integer part of divide-by number.
▒ = Bits conveying decimal part of divide-by number.
Y = Bits conveying factory-prescribed control information. *These values vary with the FN3000 version supplied.*

Figure 3: FN3000 frequency-information bitmap.

☞ The binary equivalent of the integer part is to be loaded into registers R52 and R51. The binary equivalent of the decimal part is to be loaded into registers R50, R43, R42, R41, and R40. Registers R53 down to R50 are to be loaded first, followed by address 05h, and then registers R43 down to R40, followed by address 04h. Then the registers at 03h and 09h can be loaded. The access to address 00000100 (04h) causes the internal loading of the fractional-division number.

☞ To facilitate rapid frequency changes after initialization, only the two packets that convey frequency information—those addressed to 05h and 04h—need be sent to the synthesizer, in that order.

4. Timing Requirements

Figure 4 shows the corresponding timing diagram for the three-wire serial interface. *The data is clocked on the rising edge of each clock pulse.*

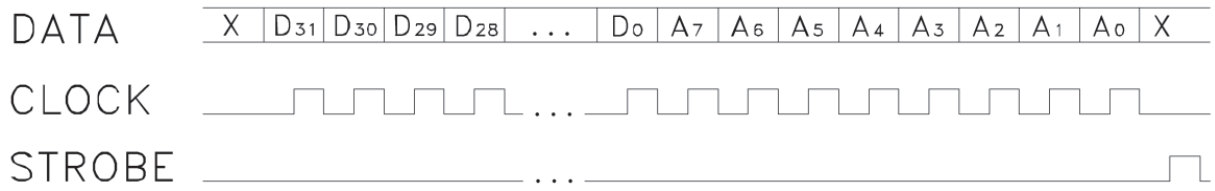

Figure 4: Timing diagram for the FN3000 serial interface.

The following timing conditions apply to the FN3000 serial interface:

Clock pulse width: 10 ns (minimum)
Data set-up time: 5 ns (minimum)
Data hold time: 5 ns (minimum)
Strobe pulse width: 15 ns (minimum)

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5. Example

The division-number calculation can be explained with the following example.

1. The desired VCO frequency F_{VCO}= 850 MHz, the reference frequency F_{ref} = 80 MHz, and the RF prescaler divisor P = 2 (factory set).

2. The reference-frequency division number R is set to one of the two factory-defined values depending upon the VCO frequency. R is changed between the two defined values to achieve the best spurious and phase-noise performance. The user is provided with a list of frequencies in Appendix 1 for which R is to be changed from the default value; in this case, the default value is 10. For frequencies listed in Appendix 1, it is to be changed to 11.

Therefore, using Equation (1):

For F_{vco} = 850 MHz with P = 2 and R = 10,

$$M = \left(\frac{850 \times 10}{2 \times 80}\right) - 1$$
$$= \frac{8500}{160} - 1$$
$$= 53.125 - 1$$
$$= 52.125$$

The data format for this example is shown in Appendix 2.
The data must be loaded as per the timing diagram (Figure 4).

Appendix 1: *R* & D5 versus Frequency (Example)

☞ The following data applies only to the example presented in Section 5, above. Consult your FN3000 documentation for the **R & D5 versus Frequency** listing specific to the model you have purchased.

1. Set R = 11 and bit D5 = 1 at address 03h for the following frequency ranges (all frequencies in MHz; step size = 1 kHz):

807.9 – 808.2
815.9 – 816.2
823.9 – 824.2
831.9 – 832.2
839.9 – 840.2
847.9 – 848.2
855.9 – 856.2
863.9 – 864.2

2. For all other frequencies between 803 MHz and 877 MHz, set R = 10 and bit D5 = 0 at address 03h.

Appendix 2: Data Format (Example)

☞ The following data applies only to the example presented in Section 5, above. Consult your FN3000 documentation for the **R & D5 versus Frequency** listing specific to the FN3000 model you have purchased.

The following is the data stream consisting of address bits **A7–A0** and their corresponding data bits for an example frequency F_{VCO} of 850 MHz based on a reference frequency F_{REF} of 80 MHz.

A7-A0	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
03h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	X	0	0	0	0	0
04h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
05h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	1	0	0	0	0	0
09h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

X = 0 for all frequencies except as listed in theR **& D5 versus Frequency** specification give

= Bits conveying integer part of divide-by number.

= Bits conveying decimal part of divide-by number.

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Fractional-N Synthesizer

SYNERGY MICROWAVE CORPORATION
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Evaluation & Test Board

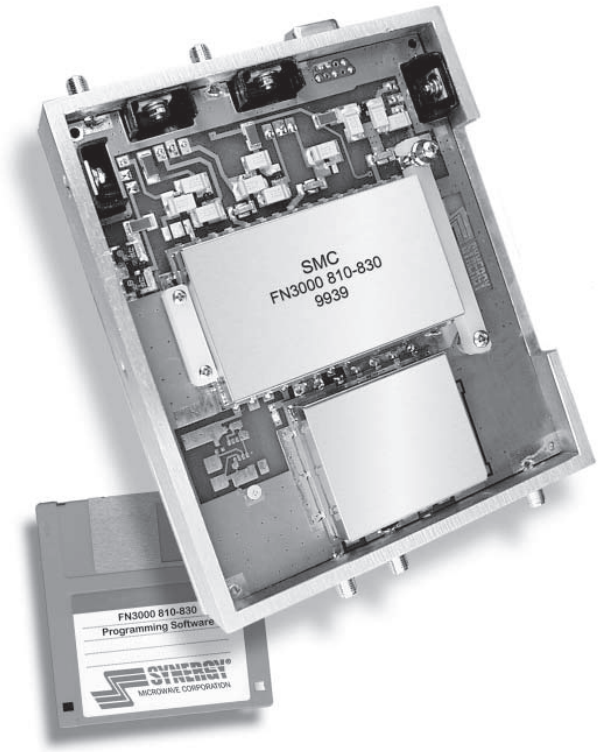
This evaluation kit contains all the hardware and software needed to experiment with a line of extremely low-noise frequency synthesizers.

Fractional-N frequency synthesizers are difficult to design, and even more challenging to evaluate. In the case of Series-3000 fractional-N frequency synthesizers from Synergy Microwave Corp. (Paterson, NJ), the evaluation effort has already been made simpler. Engineers can use the company's versatile evaluation board to "test drive" the fractional-N synthesizers with different step sizes (as small as 1 kHz), for output frequencies from 50 to 3000 MHz in various bandwidths. Ceramic resonator-based units have a typical bandwidth of 25 MHz, whereas microstrip or LC based units have been designed for optimized bandwidth and octave bandwidths.

These fractional-N frequency synthesizers (see Microwaves & RF, April, 1998, p. 151) provide switching speeds on the order of 10 µ secs and extremely low phase noise. Fractional-N synthesizers incorporating a stable ceramic-resonator-based voltage-controlled oscillator (VCO), were tested with a variety of step sizes from 1 kHz to several MHz. The high quality factor (Q) of the ceramic resonator helps to achieve phase noise of -113 dBc/Hz offset 10 kHz from the carrier, -145 dBc/Hz offset 800 kHz from the carrier, -150 dBc/Hz offset 3 MHz from the carrier.

At offset frequencies of 10 kHz (typical) and higher, the phase noise of the synthesizer is equal to that of the basic VCO. The fractional-N synthesizers cater to the need for high-dynamic range applications such as transceivers and test equipment. Ceramic-resonator-based fractional-N synthesizers with about 25 MHz tuning range are the optimum choice for narrowband base station applications such as cellular, Global System for Mobile Communications (GSM), and Personal Communications Services (PCS).

Evaluation of such low-noise synthesizers requires associated circuitry that will not degrade the synthesizer's performance. The fractional-N synthesizer evaluation board (see figure) houses low-noise power-supply (DC) conditioning and regulating circuits as well as ultra-low noise reference oscillator. Since phase noise and spurious performance depend on noise, hum, and ripple of the power supply as well as the spectral purity of the reference oscillator, the basic frequency synthesizer board already incorporates isolation circuitry for various power supplies to minimize the external influence.



The evaluation board is equipped with 120-MHz or an optional 130-MHz low-noise crystal frequency reference oscillator. This source can be phase locked to an external 10-MHz highly stable reference. With the 130-MHz reference, it can also be phase locked to 13 MHz external reference as typical for GSM applications. The board can also be ordered without the internal reference for use with an external frequency reference source, although this is only recommended when a high-performance crystal standard is available.

A fractional-N synthesizer can be tested by clamping it to the evaluation board; solder attachments are not needed. Spring-loaded contacts allow for evaluating various fractional-N synthesizer models with the same evaluation board. All ports, other than programming ports, are equipped with female SMA connectors. The programming ports are hard-wired using a flexible cable with mating connector for direct connection to the parallel printer port of a personal computer.

The rugged and reliable evaluation board is supplied with a floppy disk containing programming software for the fractional-N synthesizers. The user-friendly dos-based software runs on a standard personal computer. It allows a user to vary numerous synthesizer operating parameters, including step size, reference frequency, and output frequency during evaluation. For those needing to speed their designs to market, the circuit design and layout of the evaluation board can be readily adapted and duplicated for final system designs.

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Question: What is the difference between a conventional one-loop synthesizer and the fractional-*N* synthesizer?

Answer: The step size of a conventional synthesizer is equal to the reference frequency applied to the phase/frequency discriminator. In a fractional-division synthesizer, clever mathematical averaging inside the chip allows quasi-arbitrary frequency resolution compared to the reference frequency.

Question: What phase-noise improvement does the fractional-division synthesizer provide?

Answer: Given a single-loop synthesizer with 200-kHz reference and comparing this to a fractional synthesizer with a reference of 20 MHz, we automatically get a 40-dB improvement inside the loop bandwidth. Outside the loop bandwidth, the system reproduces the phase noise of the oscillator. The improvement achieved is 20 log (f_{out}/f_{ref}), where f_{out} is the VCO output frequency and f_{ref} is the reference frequency.

Question: Why does Synergy Microwave recommend a reference frequency of 120 MHz?

Answer: The actual reference frequency derived from the reference standard in the Synergy fractional-*N*-division synthesizer is based on the output frequency selected. We have determined that a 120-MHz crystal reference standard, divided down to a reference frequency that is selected by the intelligent system, gives the best spurious response. This mechanism, which changes the actual reference frequency as a function of the output frequency, minimizes spurious signals at the output. To get a wide range of the highest possible reference frequencies, it is desirable to use a high-frequency reference standard that on one hand is stable, and on the other hand has the best phase noise.

Question: How does the reference standard influence the phase noise?

Answer: We have found that a 120-MHz reference standard gives the most universal application and best phase-noise performance. Since the most common industry-standard reference frequencies are 10, 15, and 20 MHz, the optional evaluation board includes a means of locking its 120-MHz crystal oscillator to the signal from an external oscillator operating on one of these frequencies. The evaluation-board crystal oscillator then serves as the reference standard for the synthesizer.

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Question: What if my frequency standard operates above those three industry-standard frequencies?

Answer: Assume your frequency standard operates at 80 MHz. The easiest solution would be to divide its output by 8 and use the resulting 10-MHz signal as the reference input to the evaluation board.

Question: What if I don't want to use Synergy's evaluation board?

Answer: The phase-noise performance with your 80-MHz standard will be worse than that achievable with the evaluation board's 120-MHz reference standard. The deterioration will be 20 log (120/80), or 3.52 dB. This clearly shows the need to use as high a reference frequency as possible.

Question: Beside phase-noise performance, how will the absence of the evaluation board affect the operation of the fractional synthesizer?

Answer: The software provided with the fractional synthesizer has enough programming capabilities to adjust for your choice of reference frequency, so the synthesizer will operate properly. However, its phase-noise performance will be degraded as described above. The evaluation board also includes voltage-regulator circuitry that supplies exceptionally clean, low-noise dc to the synthesizer and reference standard. Operating the synthesizer from a noisier power source will further compromise its spectral purity.

Question: What is the best solution from a user point of view?

Answer: Since we supply the circuit diagram of the evaluation board, we recommend that users build their own equivalent of the evaluation board as a master for supply-voltage generation as well as frequency generation, taking care their board layout does not compromise the electrical performance of the circuitry. Such a board can then be used to drive several synthesizers at the same time.

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FN3000 SERIES

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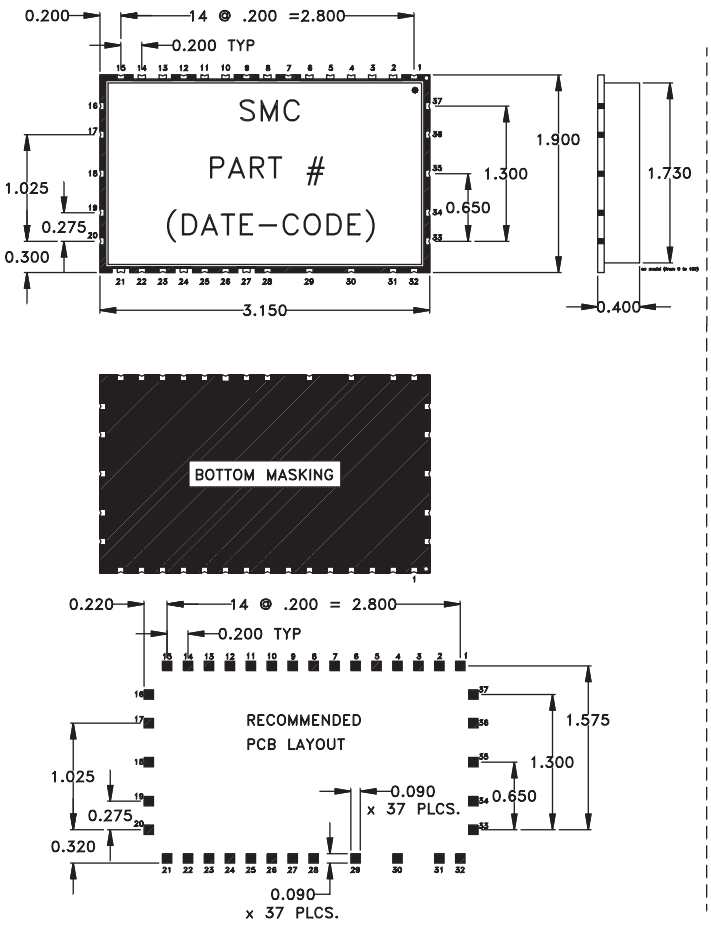

PIN OUT
2--- +5v REF ✳(Vcc1)
3--- STR-R(NOT USED)
4--- STR-S(ENABLE OR SET)
5--- SCLK(CLOCK)
6--- SDIN(DATA)
8--- +5v DIV ✳ (Vcc2)
10--- RF OUT
11--- +5v AMP ✳ (Vcc3)
13--- N/C
14--- +5v Vcc (Vcc4)**
21--- +28v (OPT.) (Vcc5)
24--- REF IN
27--- LD
ALL OTHERS GND

✳3 SEPERATE +5v SUPPLIES ARE RECOMMENDED.

✳✳ Vcc4 will vary depending on model (from 9 to 18V)

Vcc5 USED ON SOME MODELS ONLY