

Nonlinear Effects In Oscillators and Synthesizers (Invited)

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Abstract --- The proposed paper shows existing problems in VCO's and synthesizers due to the nonlinearities in the active devices and external integrated circuits. This paper proposes a design guidance on how to minimize such effects in oscillators by using nonlinear, rather than linear, tools. In synthesizers, the reference frequency and its harmonics will mix with the output frequency in the phase detector and cause spurious signals. A new method is proposed to introduce a synchronized jitter in the reference, which will move these spurious far enough outside the loop bandwidth to be suppressed by 90dB.

I. INTRODUCTION

Contrary to common discussions, oscillators, after reaching steady state, are not nonlinear in the common sense. While the collector current may show a distortion due to harmonic contents, the voltage across the resonator or even at the transistor is highly sinusoidal. The ideal oscillator exhibits a monochromatic single tone output. The noise sources, as part of the oscillator circuit, get either modulated on the carrier or the conversion characteristic of the exponential transfer properties mix noise as widebands to the carrier. The first model is a straight modulation, or AM to PM conversion. The second is a mixing property similar to a standard mixer with many frequency inputs. This "linear mixing or linear modulation" is responsible for the phase noise of the oscillator. [1]

In practice, however, even the simplest of oscillators is a VCO. This can be demonstrated by changing the supply voltage by 10% up or down and measure the frequency shift. This effect is called pushing. Responsible for this is the voltage dependent capacitance in active device, and its transfer characteristic is highly nonlinear. By adding an external diode in reverse bias condition (varactor diode or tuning diode), the frequency of the oscillator can be changed, and it becomes a voltage controlled oscillator, VCO. This tuning diode not only adds phase noise by itself, but its large signal condition can be the source of phase noise degradation. Analyzing the load lines at the output of an oscillator and looking at the negative input current and the tuning diode voltage, will give the reader a point where to start with the design.

When combining the VCO with a synthesizer, the resulting phase noise is subject to the noise sources of the synthesizer inside the loop bandwidth, and outside the loop bandwidth it will be subject to the various frequency components generated by the synthesizer. This is commonly referred to as spurious response. The latest fractional-N division synthesizers will use a wide loop bandwidth, and therefore, the actual frequency step size can be inside the loop bandwidth. This case occurs if the fractional part of the division ratio is very narrow to the carrier frequency. This requires a novel technique to jitter reference frequency resulting in spurious frequencies now far out of the loop bandwidth. This approach is also subject of this paper. [2, 3]

II. THE VCO

The VCO, in our case a common Colpitts oscillator, will operate with a medium Q resonator or a high Q resonator (ceramic resonator, dielectric resonator, YIG resonator, or other forms of high Q devices). The standard approach has been to apply the Barkhausen criteria, meaning that the forward and reverse gain, multiplied, have to be one or slightly larger, and depending on the topology, the phase shift needs to be

zero (360°) or 180°, depending on the topology of the oscillator. The Colpitts oscillator is essentially an emitter follower, and therefore, the phase shift between the base and the emitter should be zero. Fig. 1 shows such a configuration. The design guide can be seen from Fig. 1 and the calculation from (1). The two external capacitors marked C1 and C2 in reality consist of two intrinsic and two extrinsic capacitances. Linear circuit theory allows for calculation of a maximum frequency oscillation which depends upon the gain of the device and the intrinsic and extrinsic parasitics. The maximum frequency of oscillation can be quite easily determined using CAD by plotting Z_{11} with the collector at RF ground.

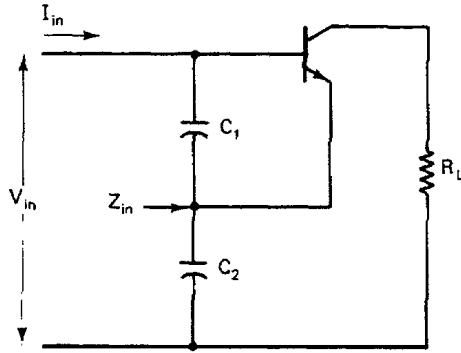


Figure 1. Input of a Colpitts oscillator; the capacitive divider generates a negative input resistance, which will start oscillation if an inductor is added.

$$R_n = -\frac{\text{Re}(Y_{21})}{\omega^2 \times C_1 \times C_2} \quad (1)$$

Fig. 2 shows the real and imaginary components of Z_{11} . For a lossless resonator, the maximum oscillation frequency occurs at the crossover point where reality of Z_{11} crosses the zero line. This is the linearized dogma. Needless to say, its incorrect. While the Barkhausen criteria in principle is valid, the large signal condition changes the voltage-dependent parameters of the transistor. All linear assumptions fail to provide the correct operating frequency unless the Q is so high (crystal oscillator) that there is no frequency pulling or pushing, or that the shunt capacitance is so large that the transistor's nonlinear contribution gets eliminated. Using a 6GHz transistor at 10MHz with large values, C1 and C2, will accomplish this. In the case of microwave frequencies, this certainly is no longer true. The linearized approach for an oscillator gives a clean curve where the reactance intercepts with zero, while the negative resistance is about at its peak. This is shown in Fig. 3.

The complete oscillators for this example are shown in Fig. 4a and Fig. 4b. Fig. 4a is a BJT transistor with DC/RF feedback in the emitter, and Fig. 4b uses a PNP transistor in the collector for DC/RF feedback. Fig. 4c shows the resulting improvement of the phase noise based on this feedback. However, let us first look at the oscillator circuit without the DC/RF feedback.

Fig. 5 shows the detailed schematic of a 5.5 to 6.6GHz oscillator. The base is "hot" because of the 1mm transmission line and the other side is grounded with a via hole. In the emitter we also have a combination of a transmission line with resonators and two tuning diodes.

Modern CAD tools allow us to investigate the load line of a transistor in an oscillator, and Fig. 6 shows the highly nonlinear operation resulting from it. Even when reducing the DC current, there is still a heavy overdrive as shown in Fig. 7. The DC current now has been reduced from 80mA to 40mA. A further

reduction of the DC, as shown in Fig. 8 reduces the overdrive condition. The DC operating bias is now about 40mA linearized and 20mA linearized. The linearization is achieved by using the DC feedback transistors, which are now part of a regular Colpitts circuit.

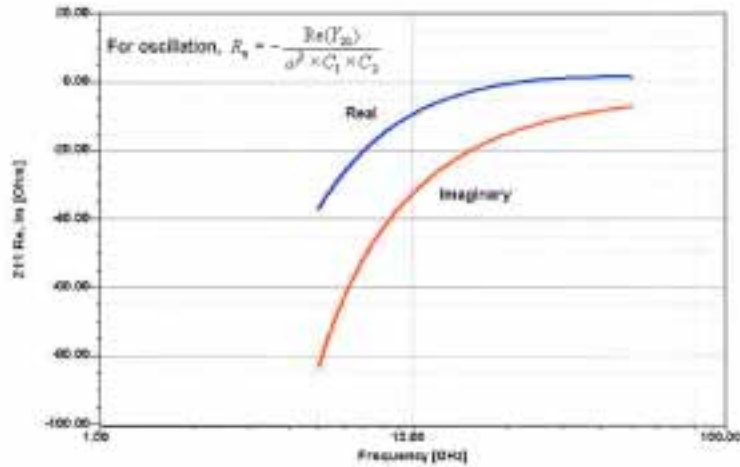


Figure 2. Real and imaginary values for Z_{11} . Real (Z_{11}) must be slightly more negative than the loss resistance in the circuit for oscillation to start. The resulting dc shift in the transistor will then provide the amplitude stabilization as g_m will be reduced.

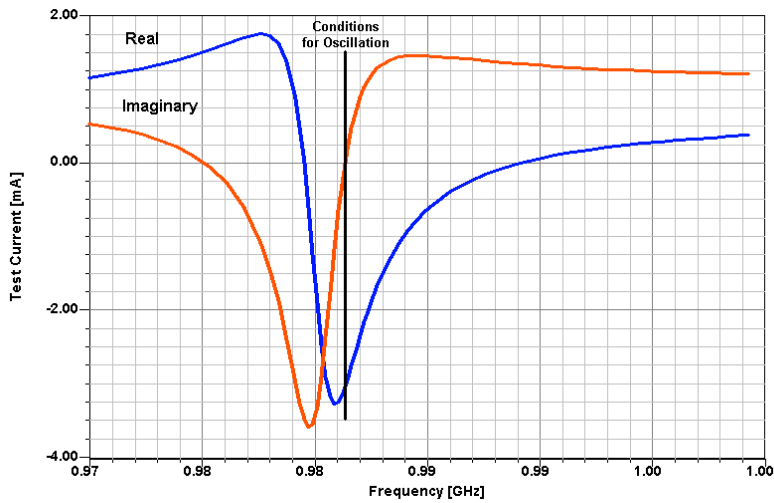


Figure 3. The steepness of the curve showing the test currents indicates a high operating Q that results in low phase noise. The steeper the slope at the changeover from inductive to capacitive reactance, the higher the resonator Q .

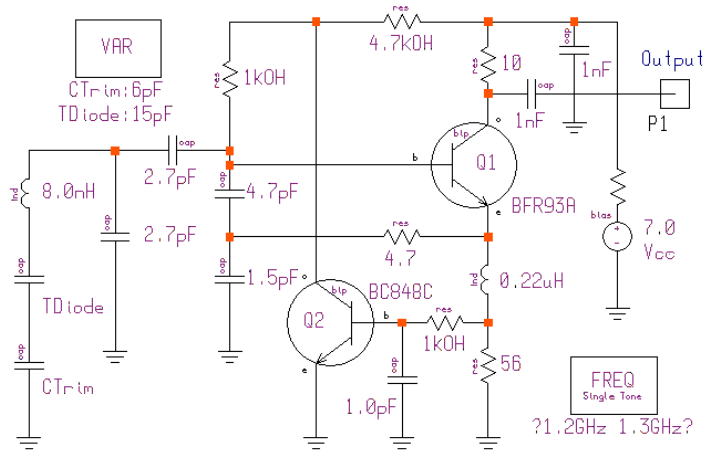


Figure 4a. BJT-based oscillator with noise feedback. The noise sampling is done in the transistor emitter. The tuning diode has been represented by a linear equivalent circuit.

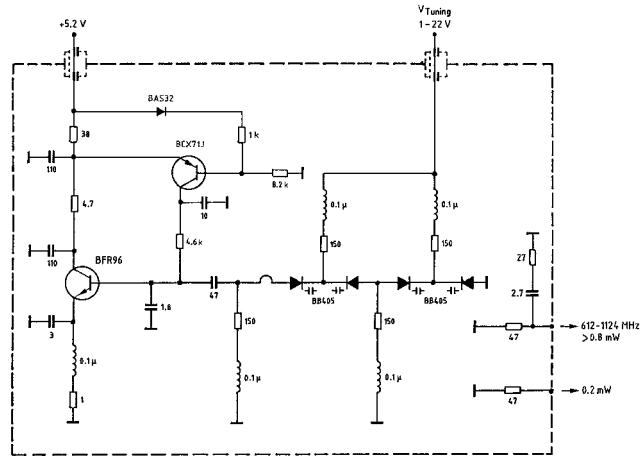


Figure 4b. BJT-based oscillator with noise feedback. The noise sampling is done in the collector. The biasing with PNP transistor has always been used for grounded emitter microwave circuits, but the feedback loop was so narrow that no noise or feedback/cancellation was possible. It uses an anti-series diode arrangement with 4 diodes.

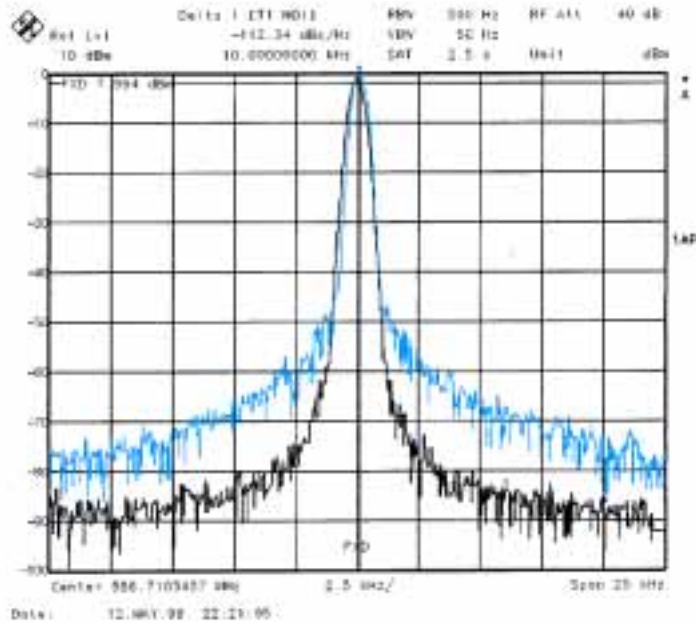


Figure 4c. Phase noise improvement caused by a novel RFIC oscillator circuit, which includes a tuning diode. However, the tuning diode coupling is only about 10MHz per volt, and therefore, does not add much to the modulation noise. For test purposes, this is an LC circuit with a loaded Q of 50 measured at about 500MHz. The IC operates up to 3GHz.

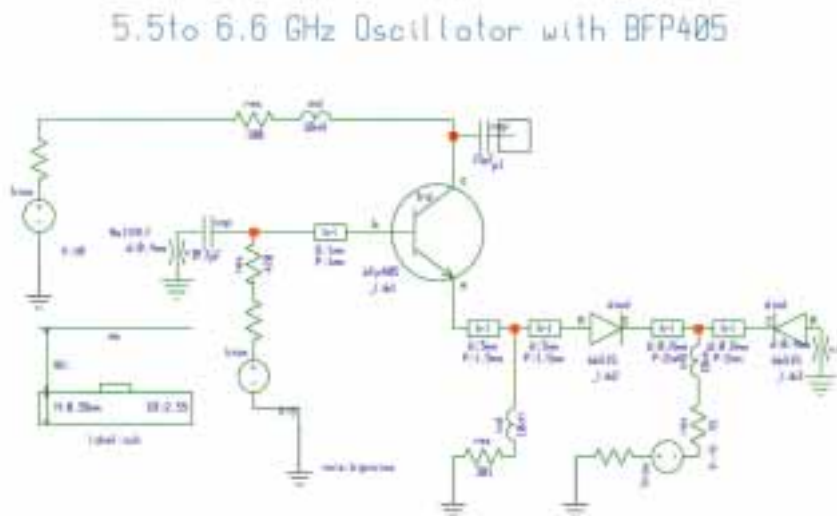


Figure 5. A 5.5 to 6.6GHz VCO using microstrip resonators. The feedback is achieved with the transmission line in the base, and the resonator consists of printed microstrip lines. This circuit follows the thoughts of [4] and [5]. It uses an anti-series diode arrangement with 2 diodes.

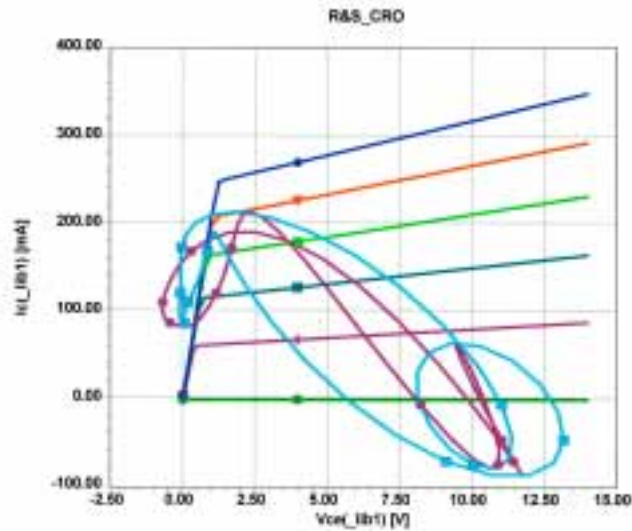


Figure 6. Output load line for 80mA collector current of a high Q resonator oscillator.

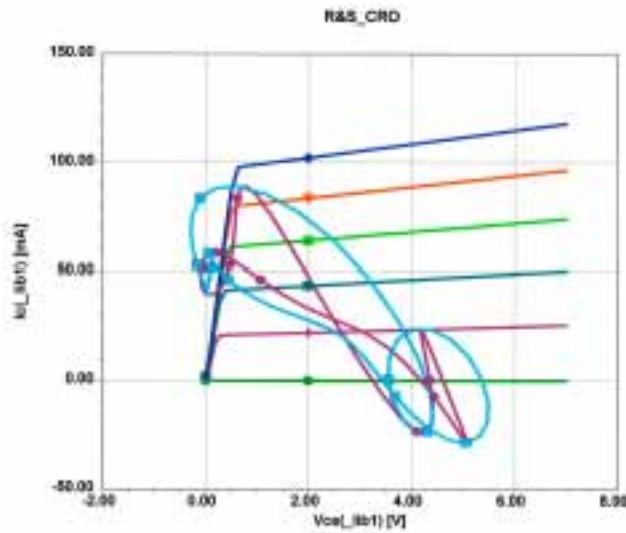


Figure 7. Output load line for 40mA collector current of a high Q resonator oscillator.

Adding tuning diodes to the circuit will immediately complicate the system. Let us assume a microwave configuration, such as shown in Fig. 8, is chosen. In this case, we actually use two tuning diodes, which is necessary to increase the tuning range beyond what one diode can achieve stable. As a result, depending on the LC ratio, we will get a picture with a very shallow resonance, such as shown in Fig. 9. This indicates a very low Q when analyzing in the linear mode. Initially, we assume that the tuning diodes have been replaced with fixed capacitors. It also shows a second resonance around 13.5GHz, but the feedback circuit is not sufficient to provide a negative resonance. Clearly, this would have been the point of best operation.

In the case of GaAs oscillators, the actual tuning diode typically can also be a gate source junction of an FET with the source and drain connected. As a side comment, silicon germanium transistors with equivalent high cut-off frequencies are beginning to penetrate the microwave applications where GaAs circuits have been dominant.

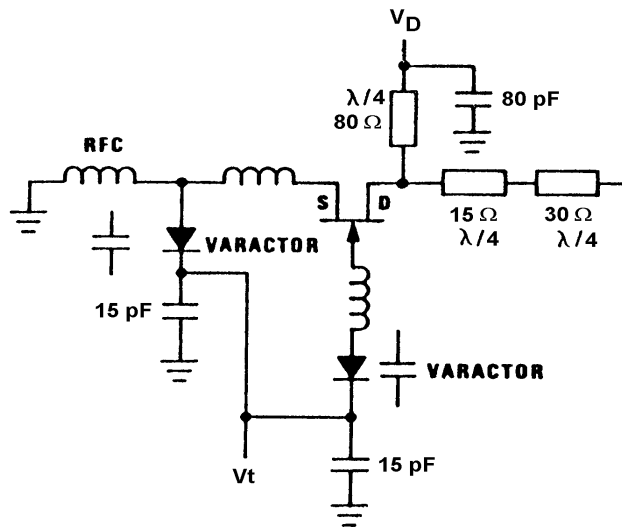


Figure 8. A simplified version of a microwave oscillator, in which the output power is obtained from the collector.

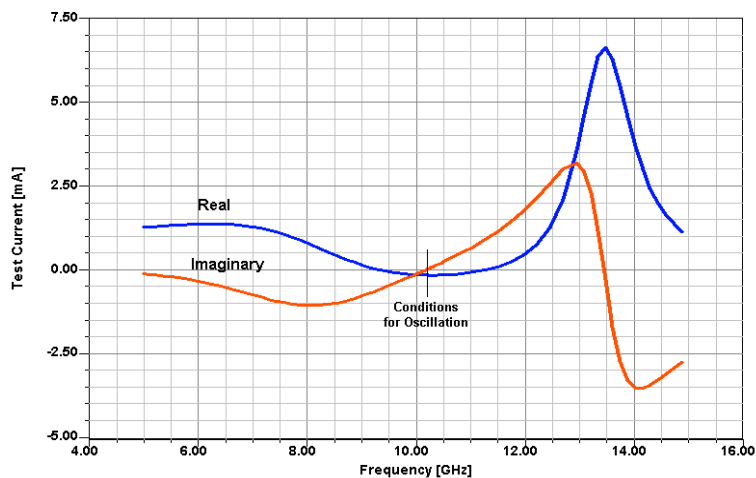


Figure 9. Display of the test currents for the LRO circuit. The imaginary curve is fairly shallow, indicating medium resonator Q . A steeper resonance, but no negative resistance, can be seen around 14 GHz; an optimized design would move this portion toward the desired oscillation frequency (10 GHz).

When connecting the tuning diodes, the smooth curve for the linear negative resistance plot, Z_{11} , expressed as a current, now shows discontinuities. In this case and for the purpose of better illustration, I have used a 47GHz oscillator in which these effects are more pronounced. The linear simulator claims an oscillator frequency of 46.3GHz. The large signal analysis will show a 47GHz actual operating frequency. However,

because of the strong linearities indicated in Fig. 10, the phase noise is not even close to what a standard Q calculation would yield.

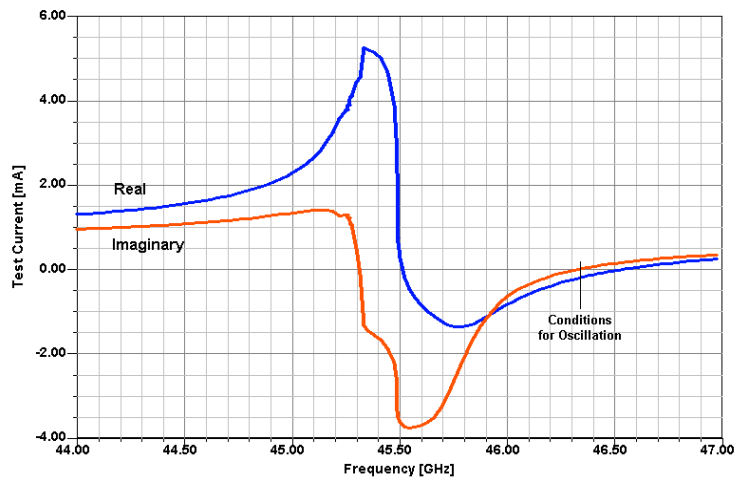


Figure 10. Test currents for finding the oscillating conditions of the 47GHz oscillator. The actual linear prediction is 46.3GHz; the large-signal condition then shifts the result towards 47GHz. The strange curves are due to the highly nonlinear operation, including the two transistors acting as tuning diodes.

Using an external AGC circuit, similar to Q2 in the previous circuit, Fig. 4a, the output load line defaults to a less violent curve. It needs to be noted that in this case neither the current nor the voltage show negative values. Needless to say, this can only be demonstrated by using a microwave simulator which has the appropriate nonlinear models, both bipolar and FET, and that the appropriate model parameters have been made available from the parameter extraction. Fig. 11 shows curves for load lines for some overdrive (left) and medium drive (right).

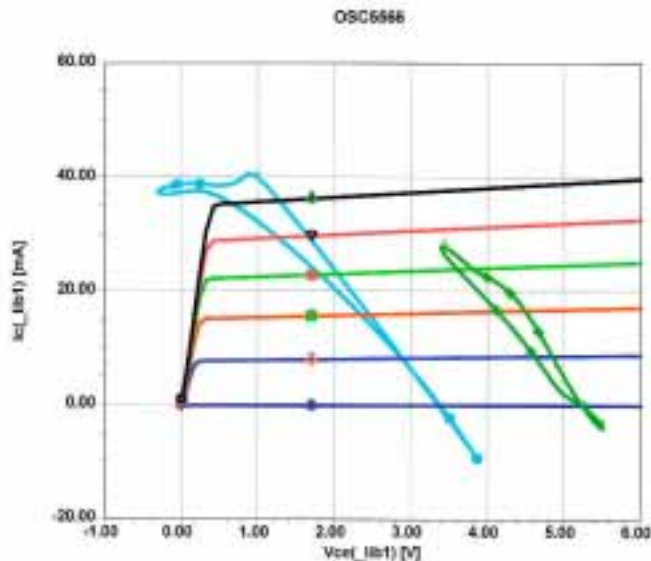


Figure 11. Load lines for overdrive (left) and medium drive (right). This circuit still exhibits negative currents.

While this AGC action reduces the output power by only 2dB, the harmonic suppression went from 4dB to about 20dB. This means that the overdrive condition was cancelled. Fig. 12 shows the harmonic power relationship between the two DC bias cases. On the other hand, the phase noise has been improved significantly, operating at a lower dissipation point. Fig. 13 shows a noise improve of almost 30dB based on this operating point. A further decrease in phase noise can be achieved if the characteristic impedance of the tuned circuit is less than 15Ω .

$$Z = \sqrt{L/C} \quad (2)$$

An even better phase noise improvement is achieved by replacing the inductor with a transmission line.

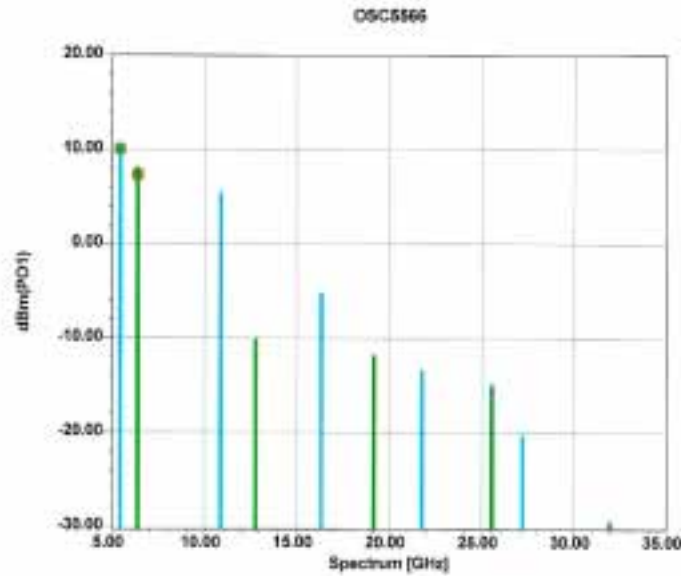


Figure 12. Reduction in harmonic controls when choosing a better (lower) bias current.

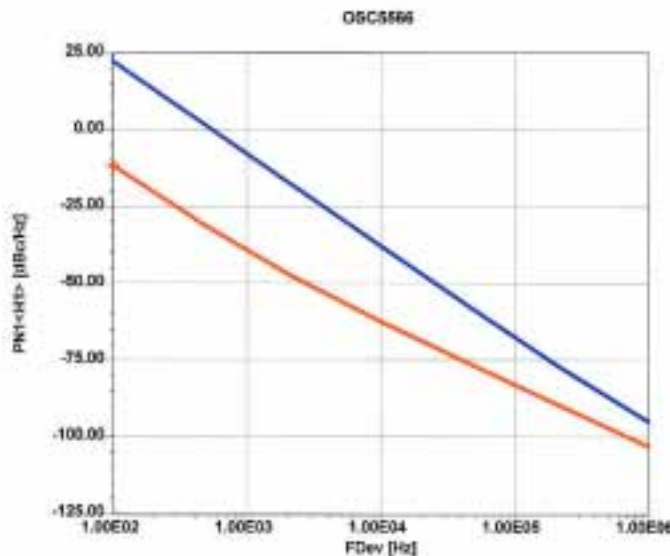


Figure 13. Noise improvement of the oscillator based on AGC action.

An additional method of reducing the second harmonic is the use of resonant capacitors in the Colpitts feedback, which provide a shunt of the harmonic components from base to ground. An international patent application for this has been filed in Europe, Asia, and the United States obtaining a wideband application. A somewhat frequency restricted form of this has been dealt with in the U.S. patent #5,144,264. Another interesting patent which was recently issued for a low noise oscillator is the U.S. patent #6,075,421, June 13, 2000. It uses a clever method of feedback, however, the purpose of having two transistors in parallel is not explained in the patent.

A good design guidance is to use a medium power bipolar transistor. Usable I_C max should be about 4-5 times the actual operating current and F_T should not be selected to be much higher than 6 times the operating frequency. The reason for the first recommendation lies in the bias dependent flicker noise, and the reason for the second recommendation lies in the fact that transistor manufacturers use stabilizing methods to make even 75GHz bipolar transistors stable at lower frequencies. This is done at the expense of low frequency noise figures, which would affect the oscillation. The flicker corner frequency increases with F_T . As to the determination of the oscillator frequency, a standard linear tool would not have shown the distortion in the test currents and even their oscillator frequency projection was incorrect. The nonlinear harmonic balance simulator was the only tool capable of delivering the frequency of oscillation within a few percent of the measured value. To be specific, the linear approach predicted 46.3GHz, while the actual measured frequency was 47GHz, which the nonlinear simulator correctly predicted.

The perfect output load can be seen in Fig. 14. This can be achieved by using a DC biased diode in the collector of an oscillator. The actual oscillator circuit uses a constant current generator, based on a hot carrier diode in the collector. The resonator used in this cases is a ceramic resonator. Fig. 15 shows the schematic of this arrangement. The resulting phase noise is extremely good. Fig. 16 shows the preliminary results based on accurate modeling. The difference between the two curves is a different bias point of the hot carrier diode. While one bias point reduces the close-in phase noise, the output power is also reduced, while the higher close-in phase noise results in a better far-out phase noise above 3MHz.

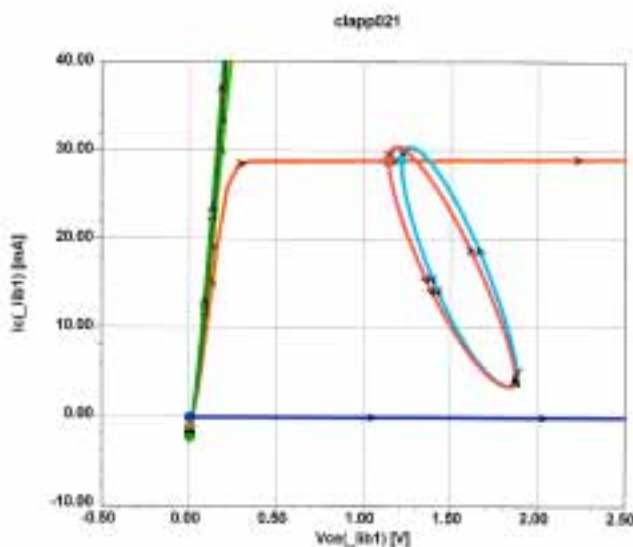


Figure 14. Perfect load line because of AGC (DC-AC linear control)+ control.

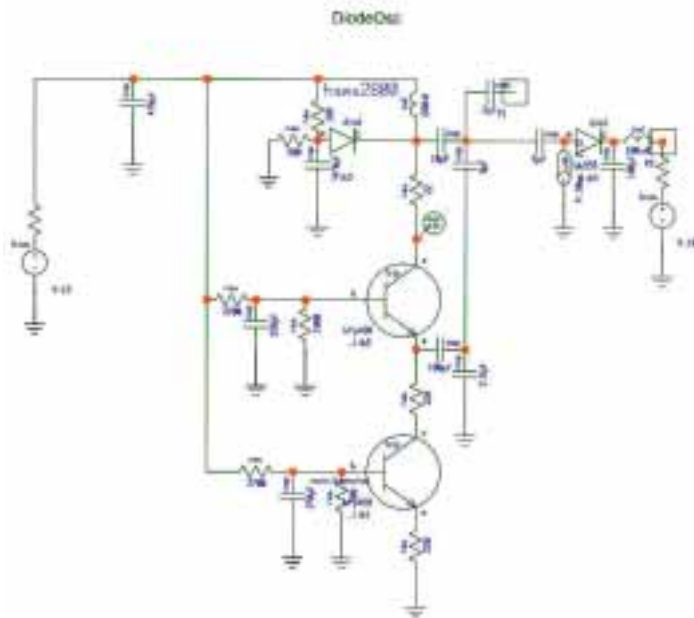


Figure 15. Ceramic resonator-based oscillator with hot carrier diode supplementing RF current which yields to better phase noise.

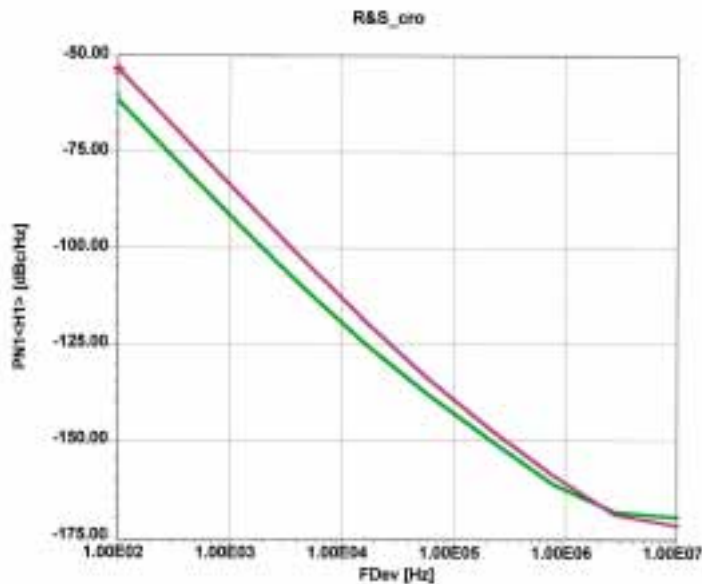


Figure 16. Predicted phase noise for two different bias points of the hot carrier diode in the collector.

As far as the biasing of the tuning diode is concerned, Fig. 17 shows a disproportionately large RF voltage across the diode. By changing the RF voltage compared to the DC voltage, and using anti-series diodes, a better result is possible. As an example, Fig. 18 shows the tuning diode AC load line for three cases of bias. Fig. 19 shows the resulting phase noise of a sample oscillator where the original application of the diode

allowed DC currents from an RF voltage, which exceeded the tuning voltage by using anti-series diodes and reducing the coupling. The results, Revision 1 and 2, can be observed.

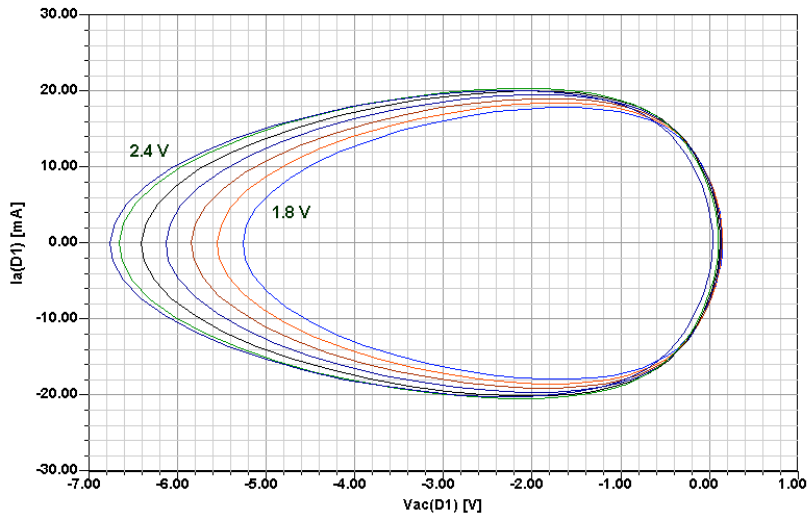


Figure 17. Graphing the tuning diode's AC load line reveals that increasing the diode's tuning bias (decrease its capacitance) results in a disproportionately large increase in the RF voltage across the diode. At all tuning voltages, the RF voltage across the diode is slightly positive (relative to the anode) during part of each cycle.

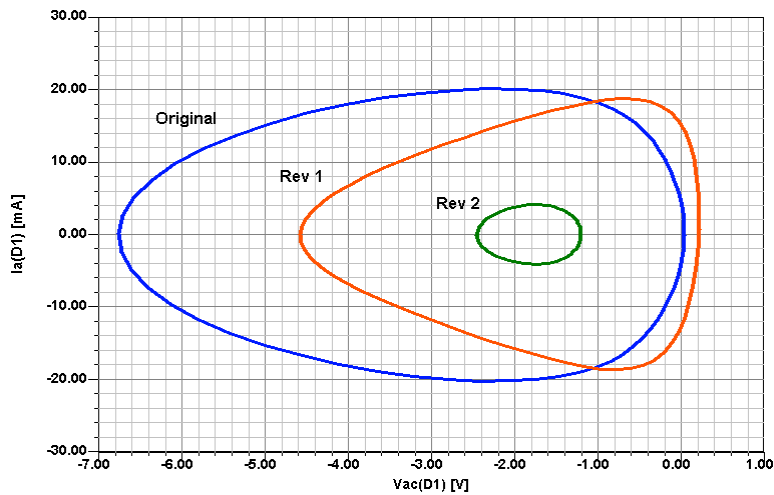


Figure 18. Comparison of the tuning diode's AC load line for the worst-case phase noise curves of Fig. 19.

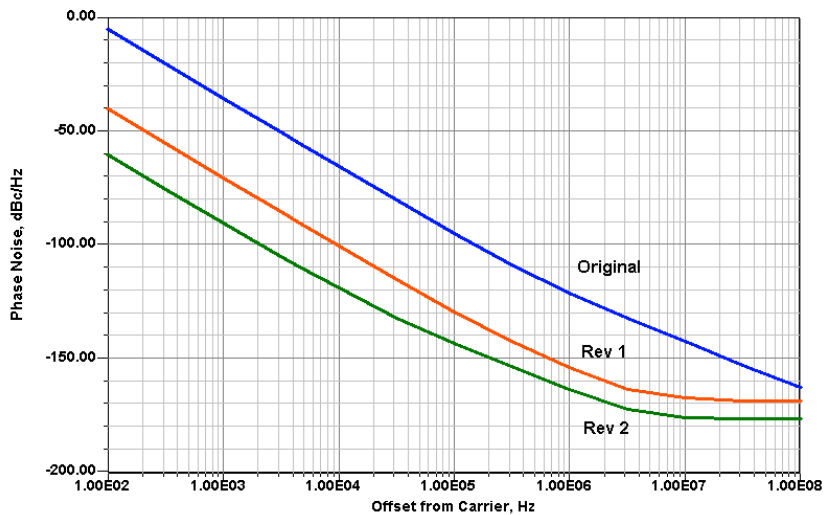


Figure 19. Comparison of worst-case phase noise performance obtained from switching from a single diode to an anti-series connection (Rev 1) and to looser coupling (Rev 2).

It goes without saying that these analyses can only be done with a nonlinear harmonic balance simulator; a linear approach, as frequently published, will not provide any insight into these.

III. NONLINEAR EFFECTS AND SPURIOUS IN SYNTHESIZERS

Traditional synthesizers using integer division ratios rarely generate spurious inside the loop bandwidth as the loop bandwidth is always narrower than the sampling frequency. Even so, there is a contradiction in designing the phase frequency discriminator because the faster they can operate (higher cut-off frequency of the gates), the more they can act as high performance mixers collecting spurious responses, and therefore, perform poorly. In the case of fractional-N division synthesizers, the loop bandwidth needs to be made as wide as possible to obtain fast switching and yet the step resolution can easily produce spurious inside the loop bandwidth. The traditional synthesizer has a step size equal to the division ratio, while the fractional-N synthesizer has an integer division and a fractional portion. It's the fractional portion which then can be inside the loop bandwidth. The traditional method of the spurious removal in a fractional-N synthesizer is a digital implementation of a cancellation technique and the use of a $\Sigma\Delta$, which pushes the noise far out.

Fig. 20 shows a block diagram of an advanced universal fractional-N synthesizer. The frequency limitation of this is really only given by the dual modulus prescaler. The implementation of the high resolution fractional-N synthesizer is achieved by a dedicated chip. Fig. 21 shows a block diagram of this chip. The frequency resolution for non-integer values is solely determined by the length of the accumulators, and the final phase noise, and spurious contents depends on the quality of the oscillator outside the loop bandwidth, the phase noise of the reference, the phase noise of the phase frequency discriminator, all associated dividers, operation amplifiers, and the power supply. The other sources of spurious are typically generated by pickup, lack of shielding, and ground loops. A good way of avoiding this is to use, where possible, separation between analog and digital circuits. Another common mistake is to set the level of integration surrounding the phase frequency discriminator to high. This results in high levels of cross-talk and one can lose as much as 10 or 15dB in performance. I have seen cases where a standard calculation would indicate 120dBc/Hz inside a 50KHz loop bandwidth and yet the achievable numbers were only 105dB and the rest was quantization noise.

Fig. 22 shows a complete schematic of a high performance, better than 1Hz resolution, fractional-N synthesizer. Its frequency limit is only determined by MC100EL32.

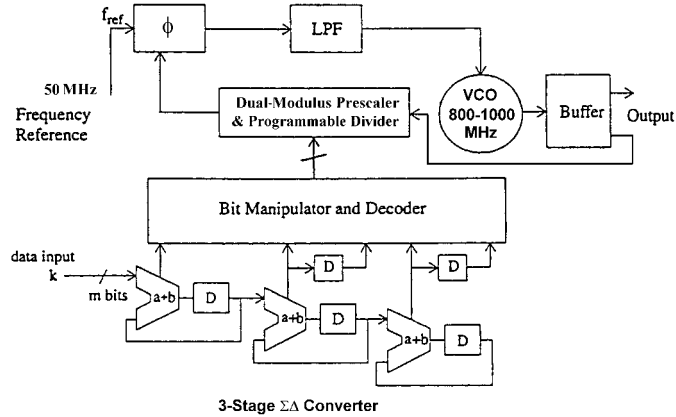


Figure 20. Block diagram of the fractional-N synthesizer built using a custom IC capable of operation at reference frequencies up to 150 MHz. The frequency is extensible up to 3 GHz using binary ($\div 2, \div 4, \div 8$, etc.) and fixed-division counters.

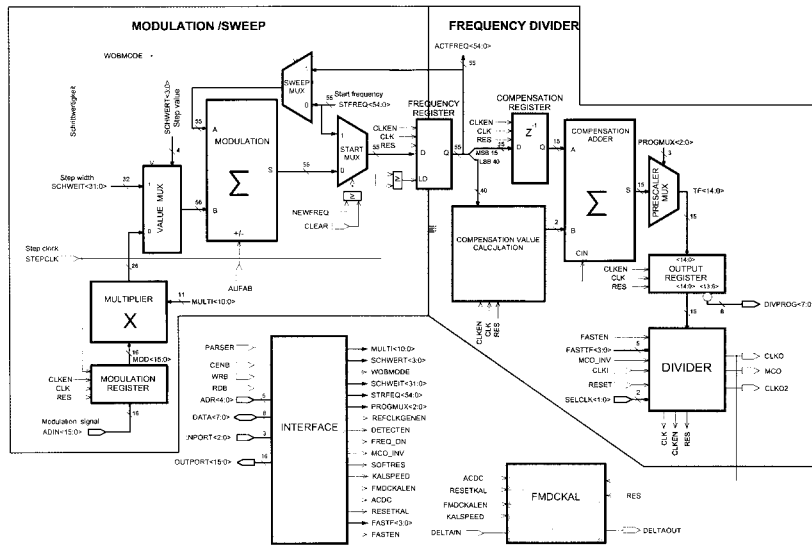


Figure 21. Detailed block diagram of the inner workings of the fractional-N-division synthesizer chip.

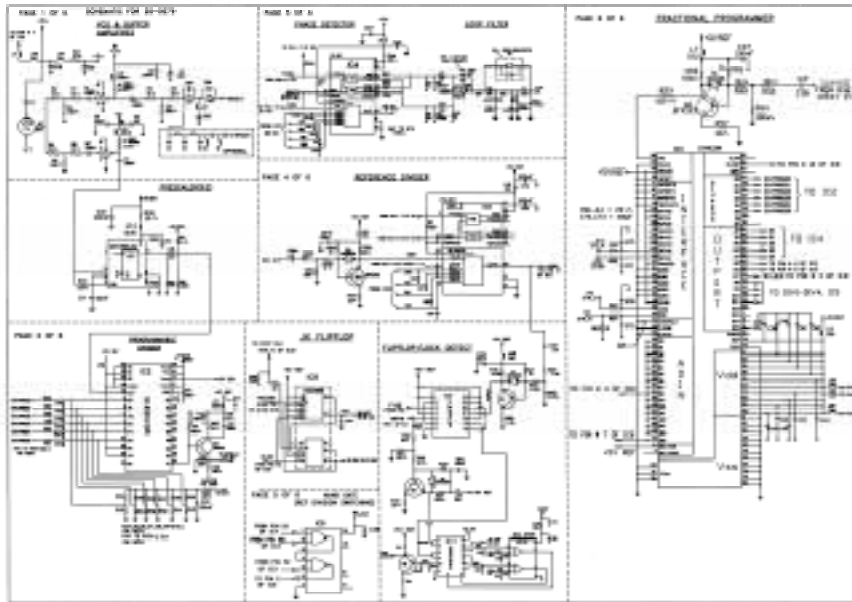


Figure 22. Detailed schematic of a fractional Division-N synthesizer with 1E-6Hz resolution. It can be driven both serial and parallel.

The main limitation of the phase noise of the synthesizer is the master standard. Fig. 23 shows a crystal oscillator specifically developed for these applications, which also shows the improvement based on the use of the hot carrier diode. This circuit uses a high Q, a 120MHz crystal with its equivalent circuit shown. Fig. 24 shows the predicted phase noise with and without the diode, which agrees quite well with the measured data, less than 2dB deviation. I found that very few companies are capable of producing this crystal with a suitable dynamic capacitor values so it can be pulled and synchronized against the master standard and at the same time have no unwanted spurious oscillations close to the carrier. At high temperatures, inexpensive crystals will show a jump to nearby unwanted resonant frequencies and show poor phase noise. In order to evaluate the performance of the synthesizer, a good universal program is needed. Fig. 25 shows an in-house tool, developed at Rohde & Schwarz, which can handle both noise and spurious products for single and mixing loop PLL's using digital compensation techniques. In this case, it analyzes a 10MHz crystal oscillator with measured phase noise and a 2000MHz VCO also with measured phase noise. Since the compensation principles have been researched for a long time and many patent applications have been filed, it is necessary to test digital compensation schemes, which are not covered by these patents, in software. A specific software tool has been developed and is shown in Fig. 26. It allows to "play" with coefficients to properly simulate both compensation schemes as well as the influence of the $\Sigma\Delta$ converter. The fractional-N principle now allows arbitrary resolution.

In the previously shown architecture, resolutions down to 1E-6GHz are possible.

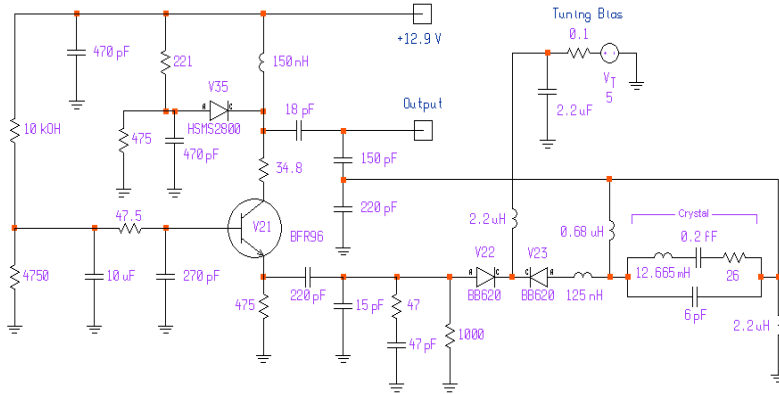


Figure 23. 100 MHz VCXO suitable for ultra-low-phase-noise applications. The HSMS2800 hot-carrier diode provides noise reduction.

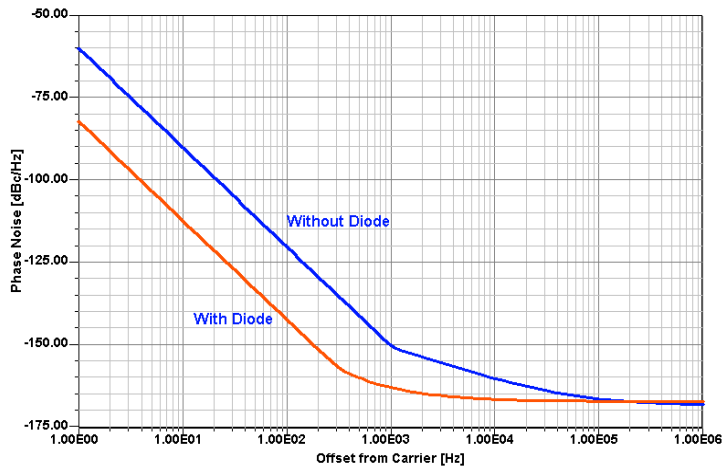


Figure 24. Phase noise of the VCXO with and without the noise-reduction diode.



Figure 25. Universal synthesizer software screen image with the various contributions as explained in the above text. It can handle single loop synthesizers multi-loop synthesizers, including up multiplication ($N < 1$) and marked as divider in mixer path. Finally, it also allows to calculate the spurious contents using the fractional synthesizer principle based on the digital compensation scheme. This is done in a separate portion of the software.

If N takes on fractional values the output frequency could will be changed in fractional increments of the reference frequency. Although a digital divider cannot provide a fractional division ratio, ways can be found to accomplish the same task effectively. The most frequently used method is to divide the output frequency by $N + 1$ every M cycles and to divide by N the rest of the time. The effective division ratio is then $N + 1/M$, and the average output frequency is given by

$$f_o = \left(N + \frac{1}{M} \right) f_r$$

This expression shows that f_o can be varied in fractional increments of the reference frequency by varying M . The technique is equivalent to constructing a fractional divider, but the fractional part of the division is actually implemented using a phase accumulator. The phase accumulator approach is illustrated by the following example.

Example: considering the problem of generating 899.8MHz using a fractional-N loop with a 50 MHz reference frequency, $899.8 \text{ MHz} = 50 \text{ MHz} \left(N + \frac{K}{F} \right)$; the integral part of the division N has to be set to 17

and the fractional part $\frac{K}{F}$ needs to be $\frac{996}{1000}$; (the fractional part $\frac{K}{F}$ is not a integer) and the VCO output has to be divided by $996 \times$ every 1,000 cycles. This can easily be implemented by adding the number 0.996 to the contents of an accumulator every cycle. Every time the accumulator overflows, the divider divides by 18 rather than by 17. Only the fractional value of the addition is retained in the phase accumulator. If we move

to the lower band or try to generate 850.2MHz, N remains 17 and $\frac{K}{F}$ becomes $\frac{4}{1000}$. This simple method of using fractional division was first introduced by using analog compensation to reduce the spurious frequencies, but today it is implemented totally as a digital approach. The necessary resolution is obtained from the dual modulus prescaling, which allows for a well established method for achieving a high-performance frequency synthesizer operating at UHF and higher frequencies. Dual-modulus prescaling avoids the loss of resolution in a system compared to a simple prescaler; it allows a VCO step equal to the value of the reference frequency to be obtained. The dual modulus prescaler then divides by N or N+1 depending upon the state of its control. The only drawback of prescalers is the minimum division ratio of the prescaler for approximately N^2 . The dual modulus divider is the key to implementing the fractional-N synthesizer principle. Although the fractional-N technique appears to have a good potential of solving the resolution limitation, it is not free of having its own complications. Typically, an overflow from the phase accumulator, which is the adder with the output feedback to the input after being latched, is used to change the instantaneous division ratio. Each overflow produces a jitter at the output frequency, caused by the fractional division, and is limited to the fractional portion of the desired division ratio.

In our case, we had chosen a step size of 200 kHz, and yet the discrete side bands vary from 200 kHz for $\frac{K}{F} = \frac{4}{1000}$ to 49.8 MHz for $\frac{K}{F} = \frac{996}{1000}$. It will become the task of the loop filter to remove those discrete spurious. While in the past the removal of the discrete spurs has been accomplished by using analog techniques, various digital methods are now available. The microprocessor has to solve the following equation:

$$N^* = \left(N + \frac{K}{F} \right) = [N(F - K) + (N + 1)K]$$

Example

For $F_o = 850.2MHz$, we obtain:

$$N^* = \frac{850.2MHz}{50MHz} = 17.004$$

Following the formula above:

$$\begin{aligned} N^* &= \left(N + \frac{K}{F} \right) = \frac{[17(1000 - 4) + (17 + 1) \times 4]}{1000} \\ &= \frac{[16932 + 72]}{1000} = 17.004 \\ F_{out} &= 50MHz \times \frac{[16932 + 72]}{1000} \end{aligned}$$

$$\begin{aligned}
&= 846.6\text{MHz} + 3.6\text{MHz} \\
&= 850.2\text{MHz}
\end{aligned}$$

The mechanism that generates the digital compensation is seen in Figure 20. This block diagram shows the approach patented by Marconi, European Patent No. 0125790B2, July 5, 1995. It consists of three first order $\Sigma\Delta$ converters which are connected in series and are responsible for a bit manipulation. Only the first accumulator is responsible for the frequency resolution, while the contents of the additional accumulators are responsible for the frequency resolution. This algorithm controls the division ratios. The systems requires a programmable divider in the loop. A simple dual modulus prescaler is not sufficient. More advanced systems incorporate the compensation algorithm digitally in the custom IC. This allows smaller division ratios than 10.

Advanced fractional-N synthesizers not only have a long accumulator, but also a very efficient spurious cancellation mechanism which is based on proprietary mathematical algorithms. This is the area of greatest research and patent application. Our software allows programming “software simulation” which will then be activated in the actual hardware. The screen image of the control software is shown in Figure 27. It accepts all the necessary values. On the top left it gets told the fractional and integer value resulting in an output frequency of 200.007MHz using the 10MHz reference. The correcting mechanism requires the entry of distortion coefficients of the phase detector and algorithm coefficients which can be entered. The values shown correspond to a particular compensation scheme. The display in the left corner shows the equivalent phase noise generated by this internal circuitry. The phase noise at the VCO is shown to be around -130dBc/Hz and then increases at $5\text{E-}2$, relative to the reference frequency. This means that the loop bandwidth (order of the PLL has to be at least three in order to suppress the quantization noise caused by the digital phase jittering, increases by 60dB/decade , using four accumulators) should be set around this value. The loop filter itself will attenuate the noise on the right side of the picture, where it can be seen that the quantization noise increases from $50\text{E-}2$. A Type-2, fourth order filter is used to achieve this. Since the linearity of the phase detector is crucial, the software checks if the chosen coefficients do not over deviate the phase detector. This is shown in the window on the right. Finally, the distribution of the compensation values also needs to be monitored as it determines overall performance.

We now take the systems software again to look at the overall result. The solid curve shows the overall phase noise including unwanted spurious results. Using the coefficients as chosen above, including the loop filter, the ultimate noise floor up to 1.05MHz is better than -140dBc/Hz reaching -180dBc/Hz at 4.5MHz . By “playing” with this coefficients, one can achieve a trade-off between the amplitude of the spurious and the cut-off of the loop. It is also possible to add additional filtering to increase the spurious suppression above 100KHz . In the case shown, the loop bandwidth was set 10KHz . The noise floor of the buffer amplifier following the reference was -165dBc/Hz , and finally, the fractional divider had a noise floor of -150dBc/Hz . The output frequency generated was 200.007MHz . This means that the fractional portion had three digits of resolution.

However, the frequency synthesizers cannot adequately reject spurious signals that appear inside the loop bandwidth. By introducing a jitter as the reference frequency, the unwanted spurious signal can be shifted far away from the loop filter so that it gets rejected by the loop filter of the synthesizer. This can be explained by the following example, where

$$\begin{aligned}
\text{Master Standard Frequency} &= 80\text{MHz} \\
\text{Reference Frequency} &= 10\text{MHz} \\
\text{Output Frequency (at the VCO)} &= 670\text{MHz}
\end{aligned}$$

Reference Division Number = 8 (integer value)

In this case the comparison frequency will be 10MHz and the fractional division number will be 67, which is an integer. Shift the frequency by 1KHz to 670.001MHz and the division will be 67.0001; which gives us a spurious signal that is 1KHz away from the carrier and -45dBc.

A novel way to circumvent this problem is to add a jitter as the reference frequency, thereby, making the comparison frequency have an integer relationship with the output frequency. This scheme can be implemented by dividing the reference frequency by 8.5, where N, A, and B correspond to 8, 1 and 2, respectively, in (3).

$$N + (A/B) = \{(B-A)N + A(N+1)\} / B \quad (3)$$

The new comparison frequency will be

$$\frac{80}{8.5} \cong 9.41176MHz$$

and the corresponding fractional division number will be approximately 71.1875, thus, providing the required frequency of 670.001MHz. It is evident that the output frequency is not close to integral multiple of the comparison frequency.

The new spurious signal will be approximately $0.5 \times 9.41126 = 4.705MHz$ away from the center frequency and be rejected by the loop filter. This spurious signal is typically 80dB down from the carrier, mostly 90dB.

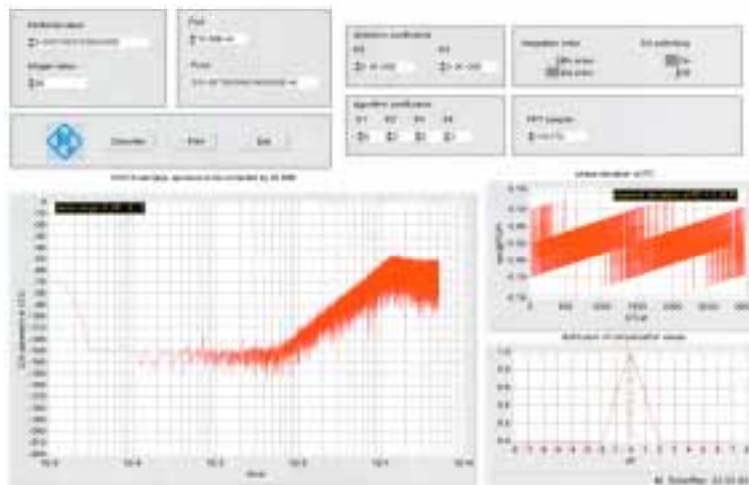


Figure 26. Simulation of a $\Sigma\Delta$ converter of the order of 4. It considers the compensation circuitry for the fractional-N synthesizer.

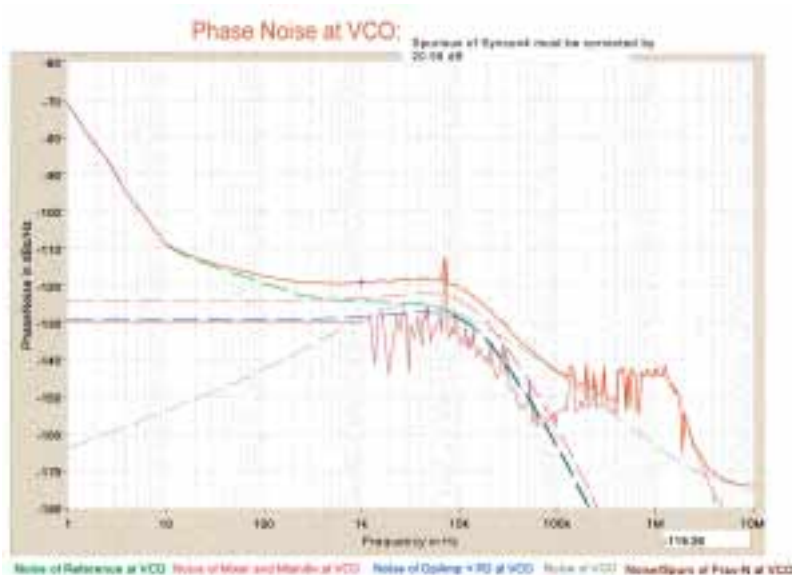


Figure 27. Composite phase noise of the fractional-N synthesizer system, including all noise and spurious signals generated within the system. The discrete spurious of 7KHz is due to the nonlinearity of the phase detector. Its value needs to be corrected by 20.58dB to a lesser value because of the bandwidth of the FFT analyzer.

IV. CONCLUSION

This paper has shown critical design parameters such as overdrive condition of the transistor, use of a DC-controlled system which can cancel phase noise, and proper use of tuning diodes. The RF voltage across the diodes must not cause any DC current to develop, and the use of anti-series diodes is essential. Further, a hot carrier diode application was shown, which reduced the phase noise significantly. In synthesizer application we evaluated the spurious mechanism and introduced a fractional-N divider in the reference part, which “jitters” the reference frequency allowing to push out the unwanted spurious frequencies.

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