

# INTELLIGENT INTERACTIVE SYNTHESIZER

## SURFACE MOUNT MODEL: FSW60170-50

**WIDE BANDWIDTH**

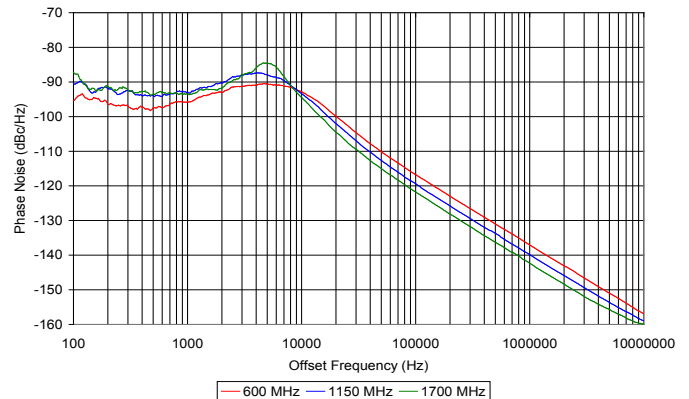
**600 - 1700 MHz**

**FEATURES:**

- ▶ Exceptionally Low Phase Noise
- ▶ Interactive Communication
- ▶ Standard Programming Interface
- ▶ Ultra Wide Tuning Range
- ▶ Lead Free - RoHS Compliant
- ▶ Patented REL-PRO® Technology
- ▶ Small Size, Surface Mount



**Phase Noise**

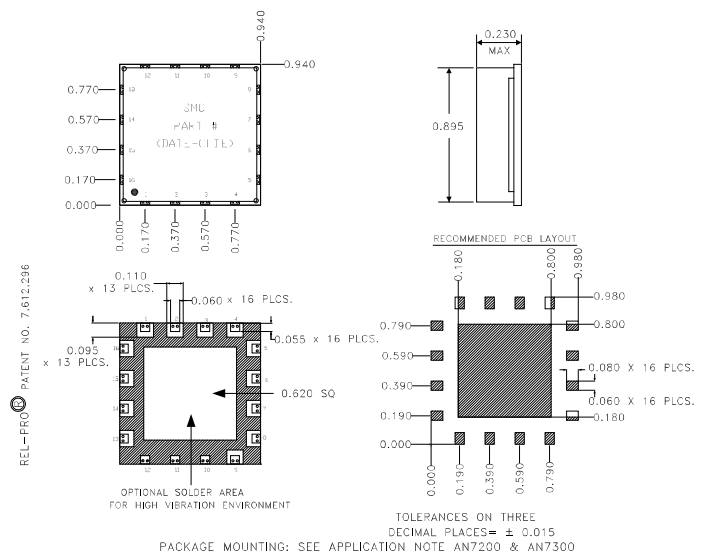


**SPECIFICATIONS (Rev. N 03/24/11)**

Frequency	600 - 1700 MHz		
Step Size	500 kHz		
Reference Input Frequency	10 MHz <sup>1</sup>		
Reference Input Voltage	1.0 V p-p to 3.3 V p-p		
Bias Voltage	<b>Vcc</b>	<b>V (Vdc)</b>	<b>I (mA Max.)</b>
	Digital	+5	15
	VCO	+5	40
	Tune	+25	10
Output Power	0 dBm (Min.)		
Spurious Suppression	85 dB (Typ.)		
Harmonic Suppression	12 dB (Typ.)		
Settling Time	10 mSec (Typ.) <sup>2</sup>		
Output Impedance	50 Ohms (Nom.)		
Lock Detect Indicator	CMOS 3.3 V		
Typical Phase Noise	<b>Offset</b>	<b>Phase Noise</b>	
	@ 1 kHz	-92 dBc/Hz	
	@ 10 kHz	-92 dBc/Hz	
	@ 100 kHz	-120 dBc/Hz	
Operating Temperature Range	-40 to +85 °C		
Programming	See Application Note: AN7100		

<sup>1</sup> Reference input frequency is programmable (See AN7100) in multiples of the step size, 10 MHz is the factory default setting. 150 MHz (Max.)  
<sup>2</sup> From the rising edge of LE to stable lock detect

**Package #** 273LF



**Absolute Maximum Ratings**

Storage Temp. Range	-55 to +125 °C
Bias Voltage (Digital)	+5.25 V
Bias Voltage (Tune)	+26 V
Bias Voltage (VCO)	+5.5 V
DC Voltage Applied to RF Out	±25 V

**Port Configuration**

Pin 1,2,3 - NC	Pin 8 - Vcc (Tune)	Pin 16 - Clock In
Pin 4 - Error flag	Pin 9 - Vcc (VCO)	All Others - Ground
Pin 5 - Latch Enable In	Pin 13 - RF Out	NC - No Connection
Pin 6 - Ref. In	Pin 14 - Lock Detect Out *	
Pin 7 - Vcc (Digital)	Pin 15 - Data In	

\* High when locked (source/sink 500 uA)

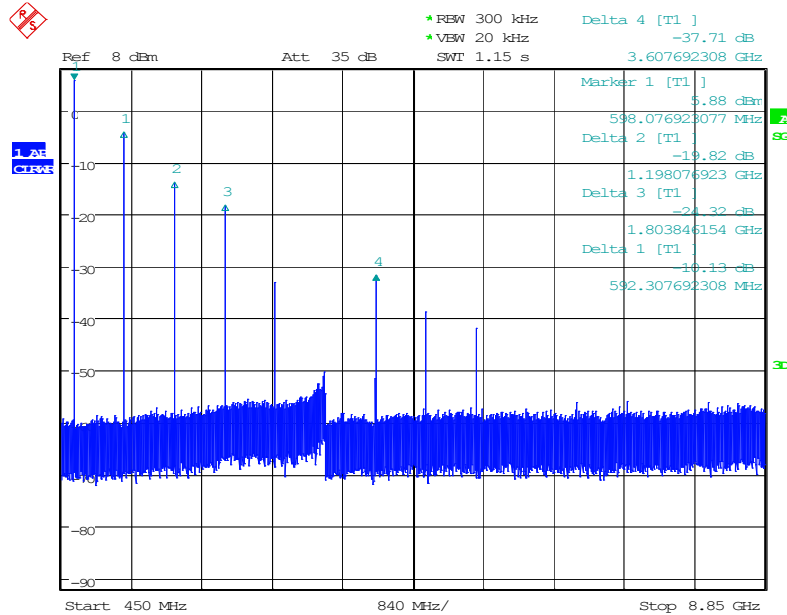
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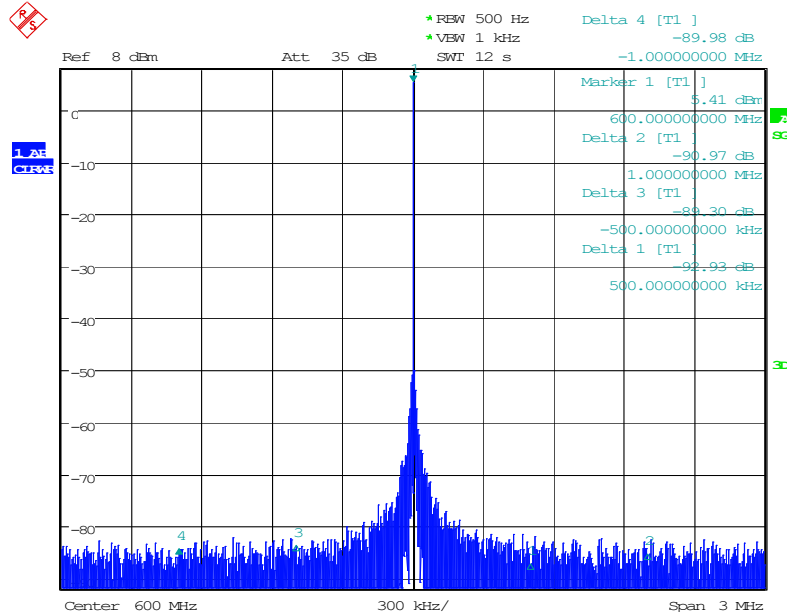
WIDE BANDWIDTH

600 - 1700 MHz

### HARMONIC SUPPRESSION



### REFERENCE SIDEBAND SUPPRESSION



PERFORMANCE PLOTS

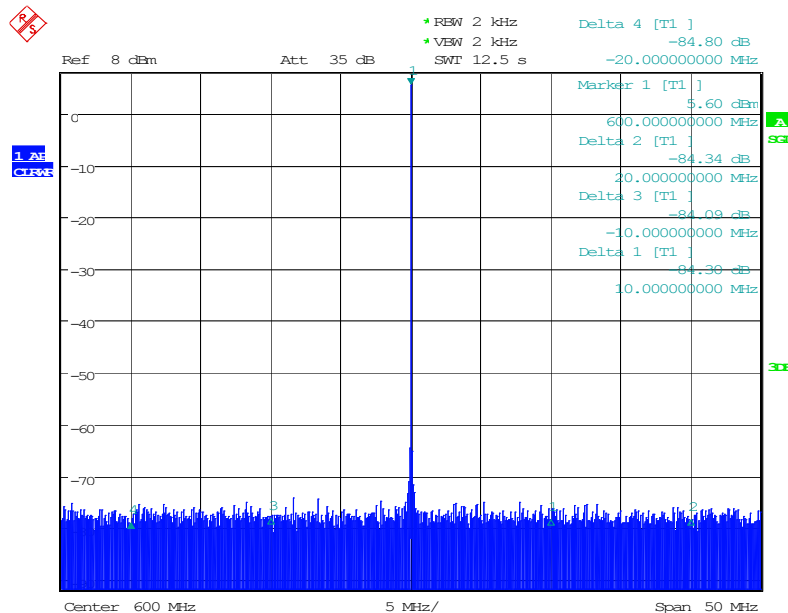
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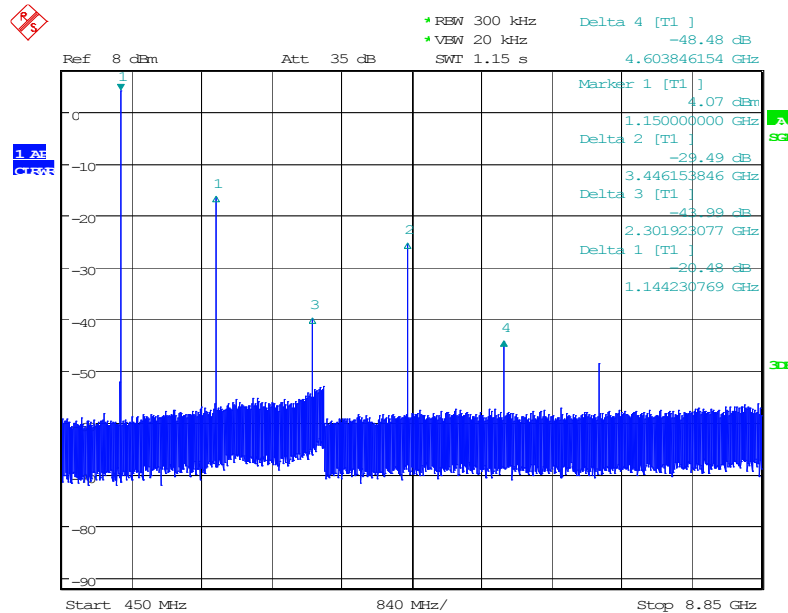
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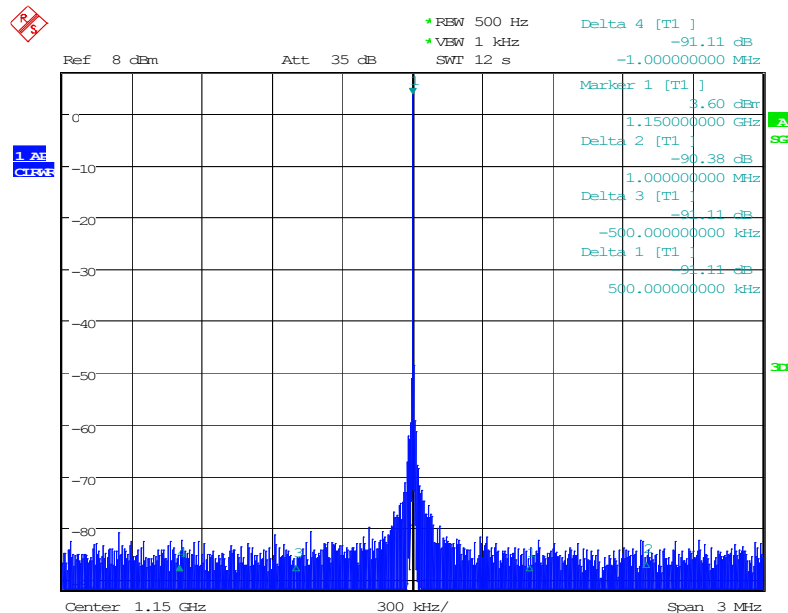
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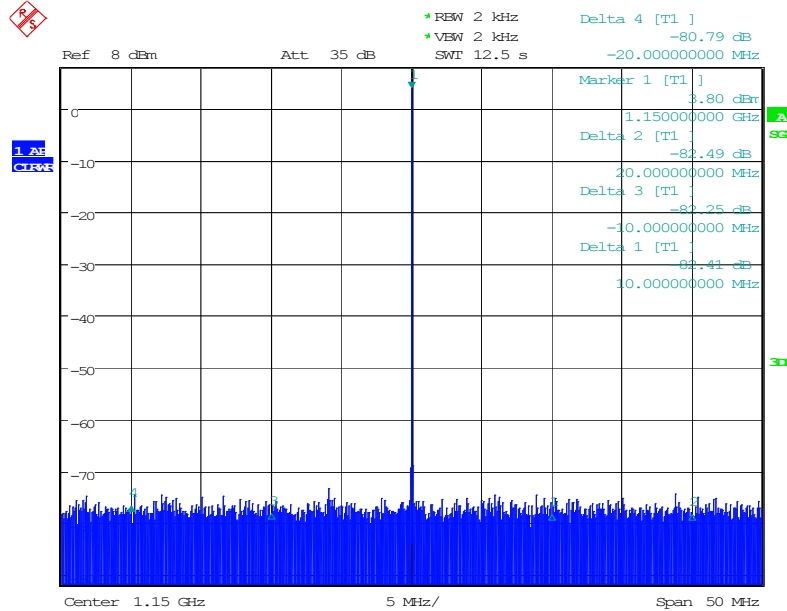
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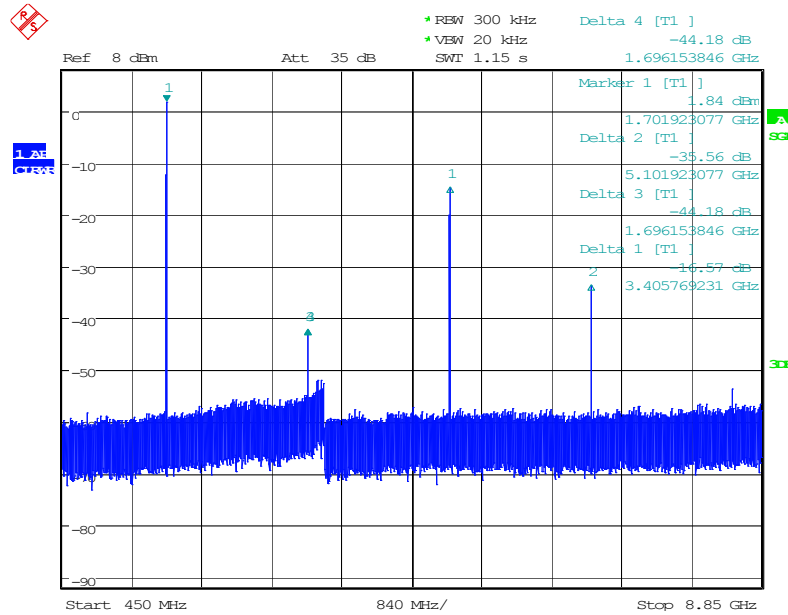
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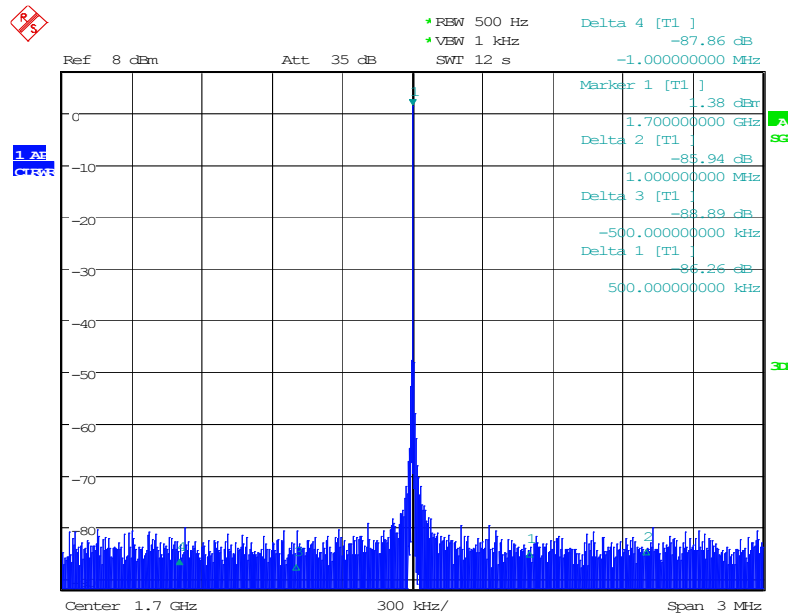
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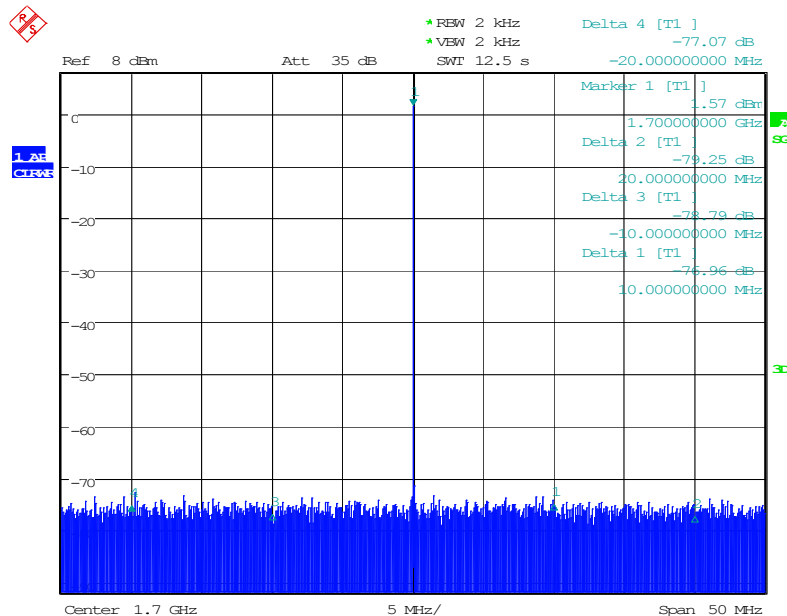
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