

# INTELLIGENT INTERACTIVE SYNTHESIZER

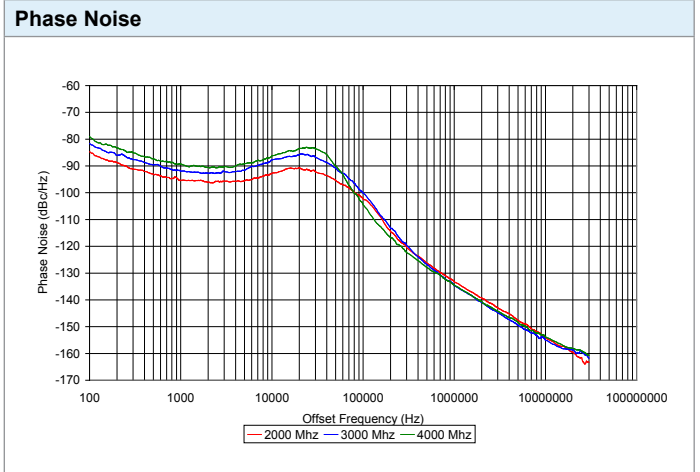
## SURFACE MOUNT MODEL: MTS2500-200400-20

WIDE BANDWIDTH

2000 - 4000 MHz

### FEATURES:

- ▶ Octave bandwidth tuning
- ▶ Small step size resolution
- ▶ Outstanding spectral purity
- ▶ High spurious rejection
- ▶ Fast lock settling time
- ▶ Easy programmable format
- ▶ Patented Rel-Pro® Technology
- ▶ RoHS Compliant
- ▶ Buffered Output



### SPECIFICATIONS (Rev B 04/22/11)

Output Frequency	2000 - 4000 MHz
Bandwidth	2000 MHz
External Reference <sup>1</sup>	20 MHz
External Reference Input	1 V p-p to 3.3 V p-p
Step Size	Programmable to 1 Hz
<b>Bias Voltage</b>	
VCC1 (VCO)	+5 VDC @ 70 mA (Max.)
VCC2 (Analog)	+3.3 VDC @ 140 mA (Max.)
VCC3 (Digital)	+3.3 VDC @ 50 mA (Max.)
VCC4 (Converter)	+5 VDC @ 45 mA (Max.)
VCC5 (Converter Output)	+25 VDC
VCC6 (PLL)	+5 VDC @ 2 mA (Max.)
VCC7 (PLL)	+3.3 VDC @ 20 mA (Max.)
VCC8 (Vtune) <sup>2</sup>	+16 VDC @ 5 mA (Max.)
Output Power	+5.5 dBm (Min.)
Spurious Suppression	50 dB (Typ.)
Harmonic Suppression	10 dB (Typ.)

<b>Typical Phase Noise</b>	Offset	dBc/Hz.
	1 kHz	-88
	10 kHz	-87
<b>Settling Time <sup>3</sup></b>	Within 1 kHz	<10 mSec
	Within 10 Hz	<20 mSec
<b>Output Impedance</b>	50 Ohms (Nom.)	
<b>Operating Temperature Range</b>	-20 to +70 °C	
<b>Non-Operating Temperature Range</b>	-40 to +85 °C	
<b>Programming</b>	See Application Note: AN7400	
<b>Programming Bus <sup>4</sup></b>	Specify SPI or RS-232	

Absolute Maximum Ratings	
Storage Temp. Range	-55 to +125 °C
Bias Voltage (+3.3 V)	+3.6 V
Bias Voltage (+5.0 V)	+5.5 V
DC Voltage Applied to RF Out	± 25 V

<sup>1</sup> Reference input frequency can be factory programmed for requested common reference frequencies from 10 - 25 MHz. Unless otherwise specified, the reference frequency is factory programmed for 20 MHz.

<sup>2</sup> If supply voltage from converter output is not used.

<sup>3</sup> Time between latch enable (LE) high (after user command) and final output frequency.

<sup>4</sup> Default bus (if unspecified) is SPI.

This product is manufactured under one or more of the following patents: Approved: 5,160,810; 5,122,621; 5,390,349; 5,416,449; 5,650,754; 5,805,431; 6,525,623; 6,850,575; 7,088,189; 7,180,381; 7,196,591; 7,262,670; 7,265,642; 7,292,113; 7,365,612; 7,495,525; 2,548,311; 2,548,317; 7,545,229; 7,580,693; 7,586,381; 7,605,670; 7,636,021; 2,533,623 | Pending: 60/493075; 60/501371 & 60/501790; 60/527957 & 60/528670; 60/563481; 60/564173; 60/589090; 60/601823; 60/605791; EV31369834; 11/259766; 60/622485 & 60/710310; 10/937525/60/736901; 60/732787; 7,495,525; 2,548,311; 2,548,317; 7,545,229; 2,563,174; 7,580,693; 7,612,296; 2,524,751

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WIDE BANDWIDTH

2000 - 4000 MHz

<b>Package #</b>	344
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REL-PRO PATENT NO. 7,612,296

TOLERANCES ON THREE DECIMAL PLACES =  $\pm 0.015$

PACKAGE MOUNTING: SEE APPLICATION NOTE AN7200 & AN7300

Port Configuration		
Pin 3 - VCC 1 (VCO = +5 Vdc)	Pin 15 - MISO (SPI)	Pin 28 - VCC 5 (Converter output = +25 Vdc)**
Pin 6 - RF Out	Pin 16 - Latch Enable (LE)	Pin 35 - GND*
Pin 8 - VCC 2 (Analog = 3.3 Vdc)	Pin 18 - Reset	Pin 39 - VCC 6 (PLL = +5 Vdc)
Pin 9 - NC*	Pin 19 - MOSI (SPI)	Pin 40 - VCC 7 (PLL = +3.3 Vdc)
Pin 10 - NC*	Pin 20 - RXD (RS-232) ***	Pin 44 - VCC 8 (Vtune = +25 Vdc)**
Pin 11 - VCC 3 (Digital = 3.3 Vdc)	Pin 21 - TXD (RS-232) ***	Pin 43, 45 - NC (No Connection)
Pin 13 - Clock (SPI)	Pin 22 - Ref In	All Others - Ground (1,2,4,5,7,12,17,23,24,25, 26,29,30,31,32,33,34,36,37,38,41,42,46,47,48)
Pin 14 - Lock Detect (LD)	Pin 27 - VCC 4 (Converter = +5 Vdc)	

\* Future expansion for modulation options (digital and analog).  
 \*\* Connect together externally and bypass with shunt 10  $\mu$ F 35 V tantalum capacitor to ground. (For applications where an external well filtered 25 volts supply is available, leave pin 27 unconnected and apply the 25 volts directly to pin 44.)  
 \*\*\* Positive CMOS level (Unbuffered).

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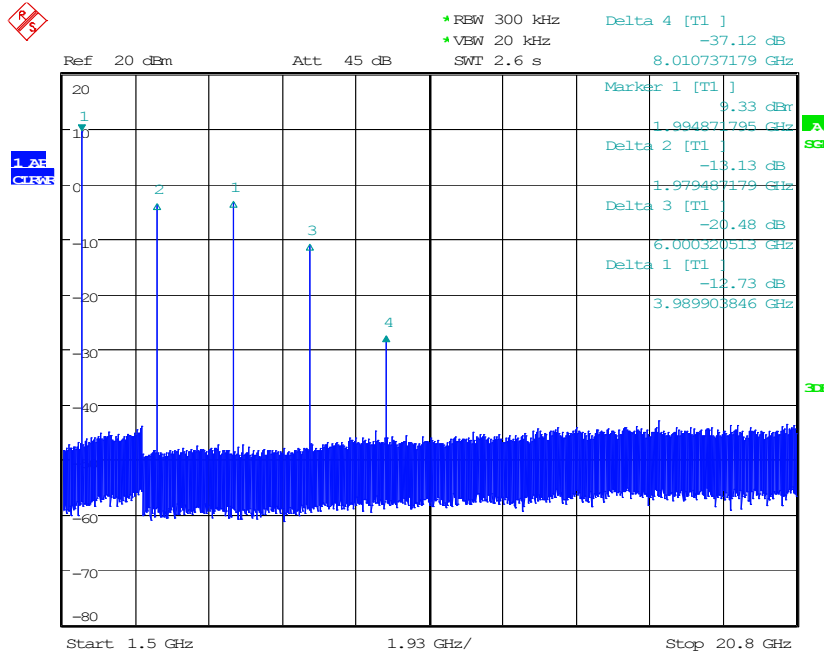
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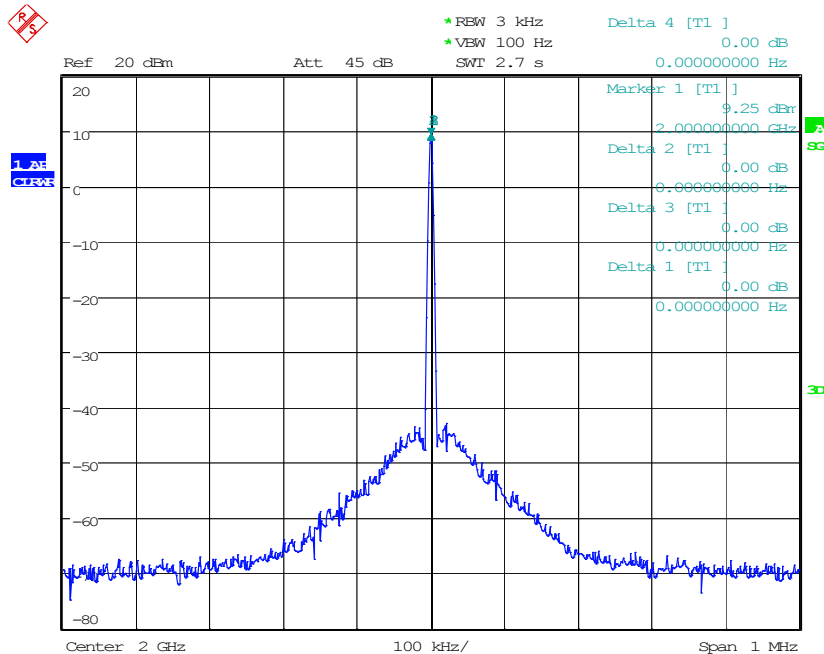
WIDE BANDWIDTH

2000 - 4000 MHz

HARMONIC SUPPRESSION



REFERENCE SIDEBAND SUPPRESSION



PERFORMANCE PLOTS

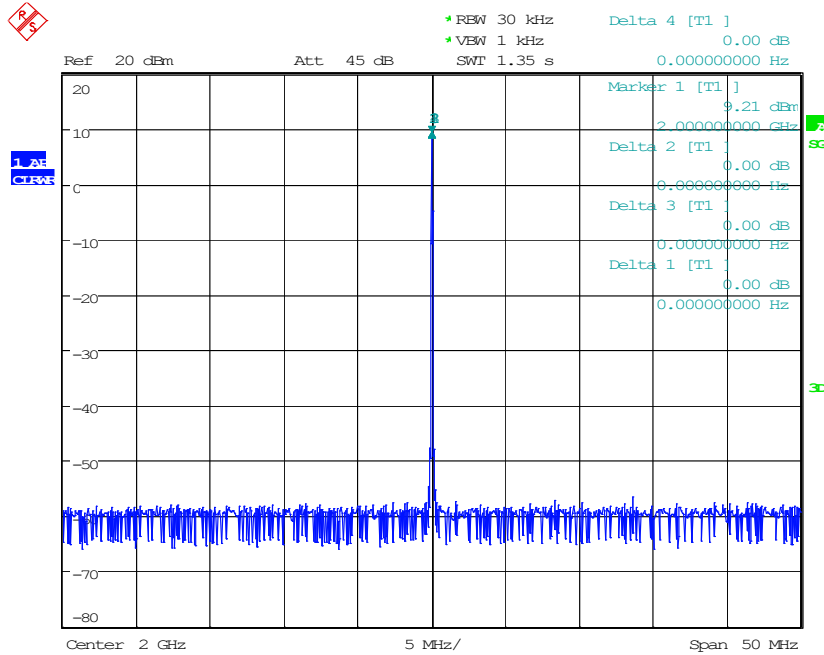
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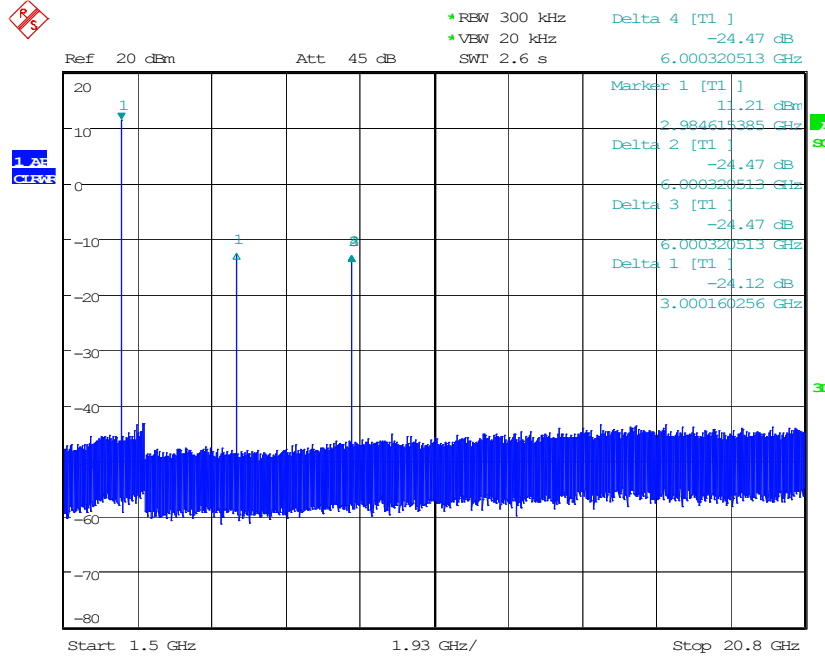


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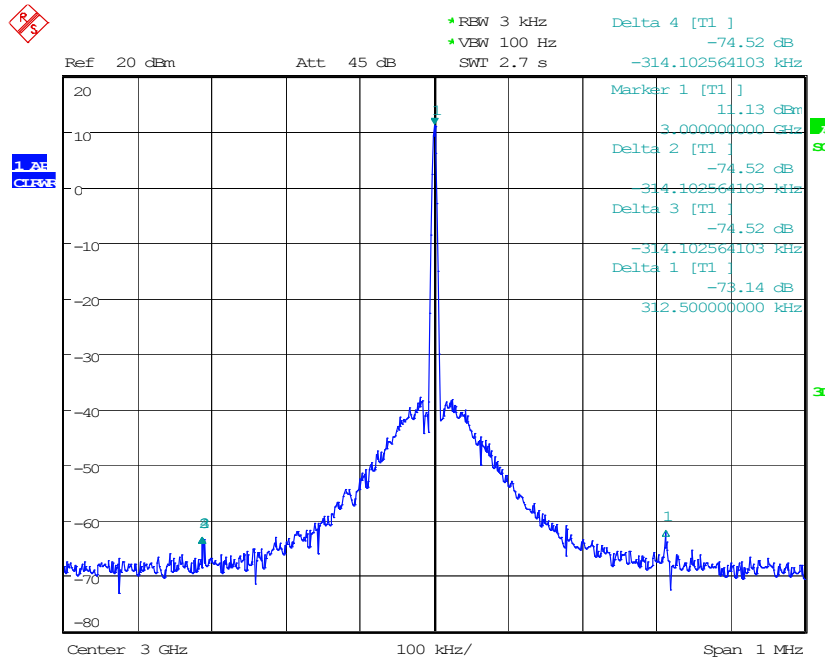
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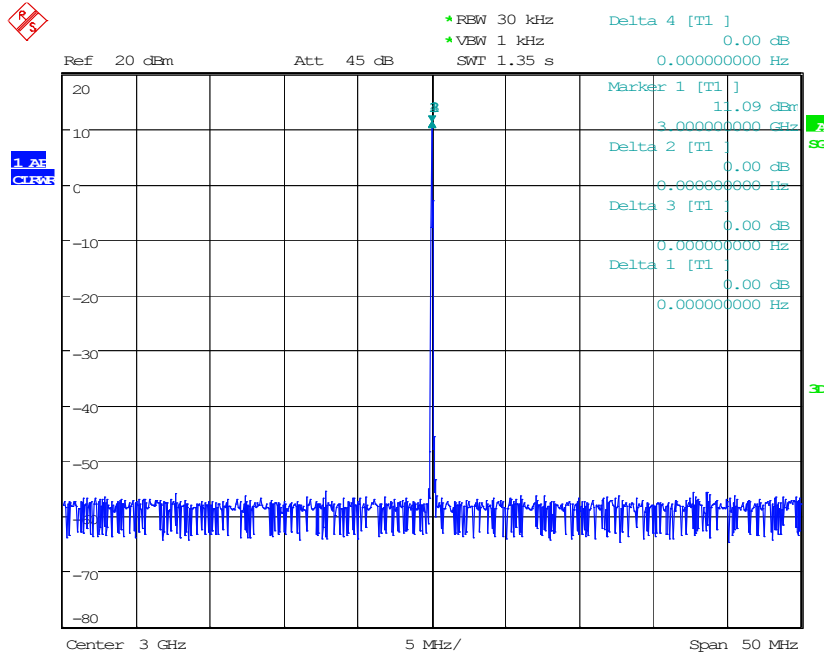
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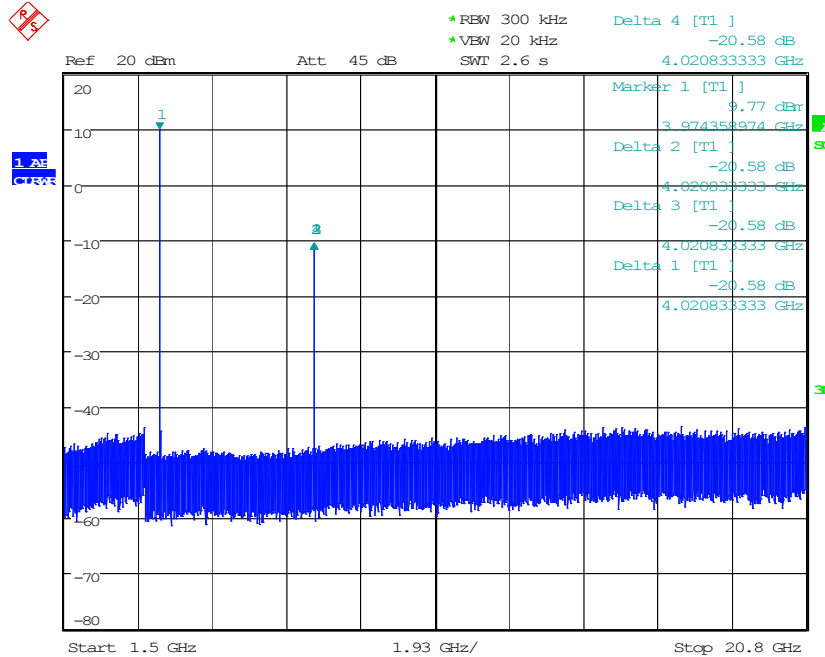
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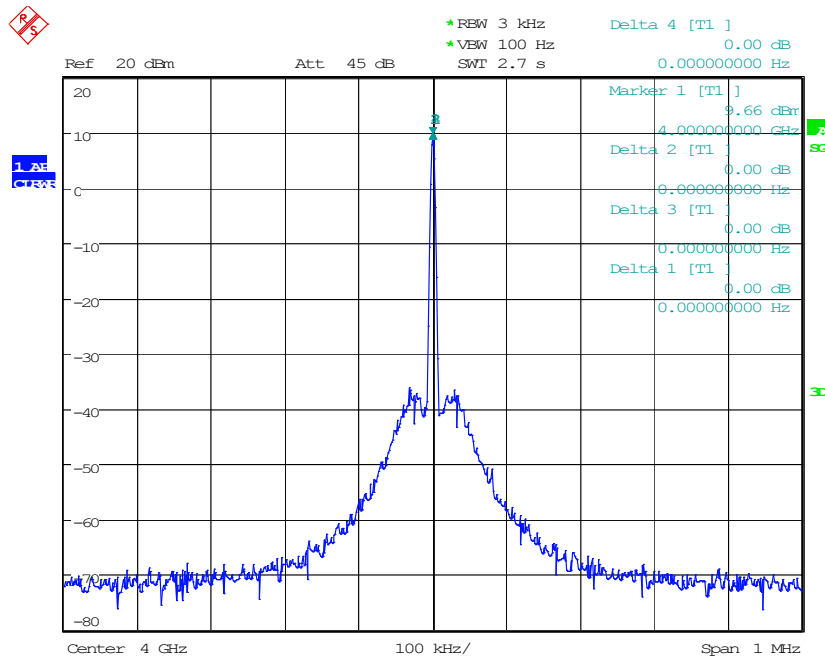
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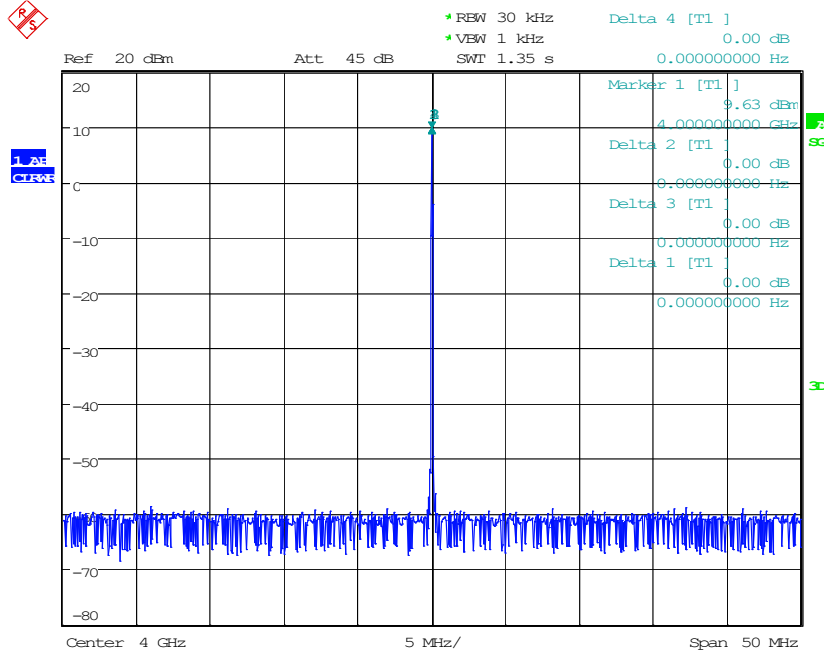
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