

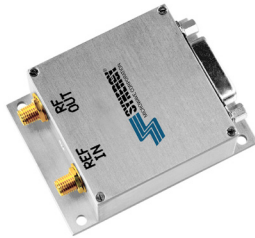
REFERENCE PHASE LOCKED TRANSLATOR CONNECTORIZED MODEL: KFCTS1000-100-5

FIXED FREQUENCY

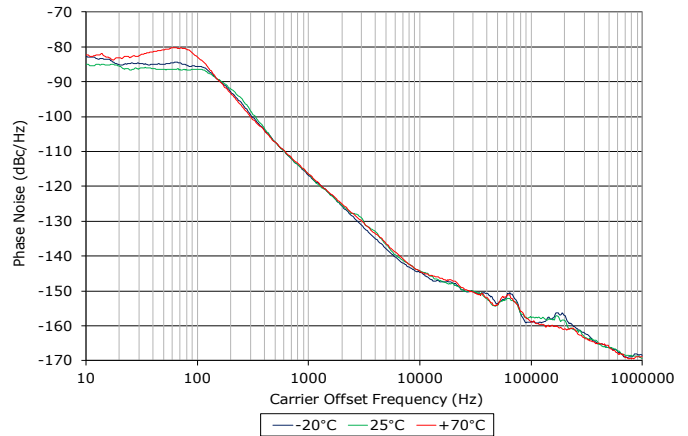
1000 MHz

FEATURES:

- ▶ Ultra-Low Phase Noise
- ▶ No Programming Required



Phase Noise (Measured with Agilent E5052A or R&S FSUP-26/27)



SPECIFICATIONS (Rev A 11/30/23)

Frequency	1000 MHz		
Reference Input Frequency	100 MHz ¹		
Reference Input Voltage	1.0 to 3.3 V p-p		
Bias Voltage	Vcc	V (Vdc)	I (mA Max.)
	Digital	+5	25
	Tune	+12	10
	VCO	+5	35
Output Power	-3 dBm (Min.)		
Spurious Suppression	80 dB (Typ.)		
Harmonic Suppression	25 dB (Typ.)		
Output Impedance	50 Ohms (Nom.)		
Lock Detect Indicator	CMOS 3.3 V		
Typical Phase Noise	Offset	Phase Noise	
	@ 100 Hz	-80 dBc/Hz	
	@ 1 kHz	-115 dBc/Hz	
	@ 10 kHz	-141 dBc/Hz	
@ 100 kHz	-158 dBc/Hz		
Operating Temperature Range	-20 to +70 °C		

¹ External 100 MHz reference sources should have phase noise better than -120 dBc/Hz @ 50 Hz offset to achieve published specifications.

Absolute Maximum Ratings

Storage Temp. Range	-40 to +85 °C
Bias Voltage (Digital)	+5.25 V
Bias Voltage (Tune)	+13.0 V
Bias Voltage (VCO)	+5.5 V

Patent : <http://www.synergymwave.com/patents>

Package # 337

PORT CONFIGURATION

Pin 1 - Vcc (Digital)	Pin 8 - Lock Detect *	NC - No Connection
Pin 2 - Vcc (Tune)	Pin 9 - Vcc (VCO)	
Pin 3,4,5,6 - NC	Pin 11,12,13,14 - NC	
Pin 7 - NC	Pin 10,15 - Ground	

* High when locked (source/sink 500 uA)

TOLERANCE: UNLESS OTHERWISE SPECIFIED .XXX ±0.015

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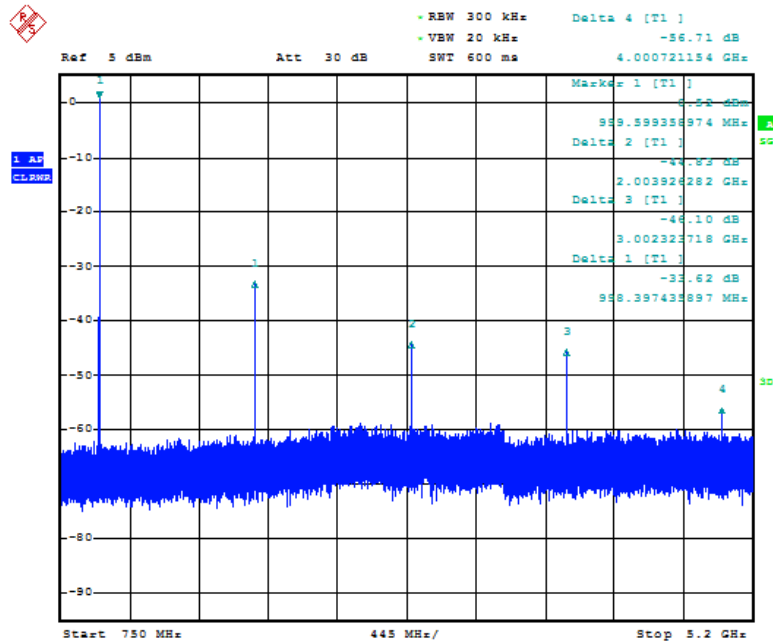
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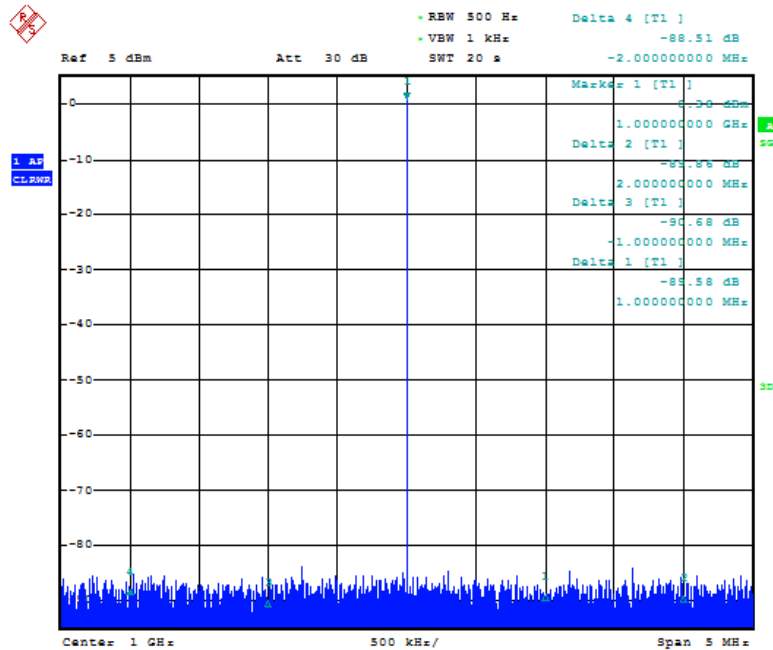
@ -20 °C

PERFORMANCE PLOTS

HARMONIC SUPPRESSION



REFERENCE SIDEBAND SUPPRESSION



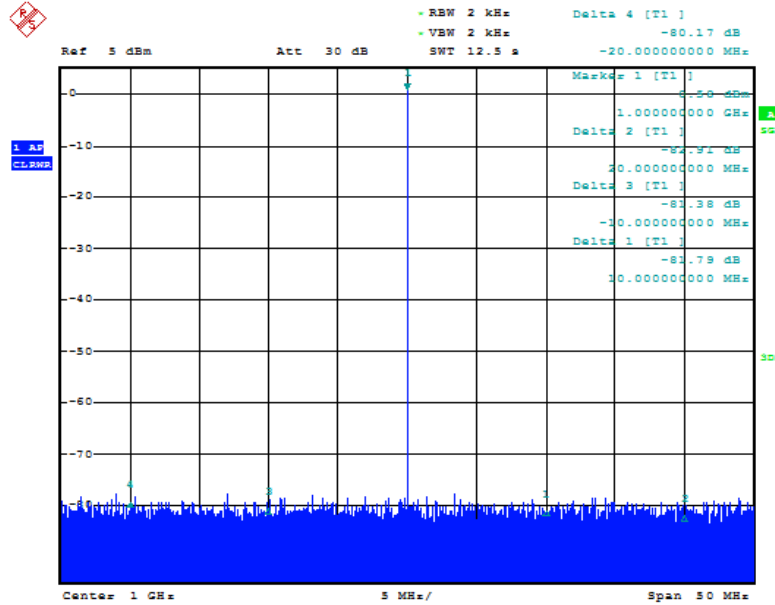
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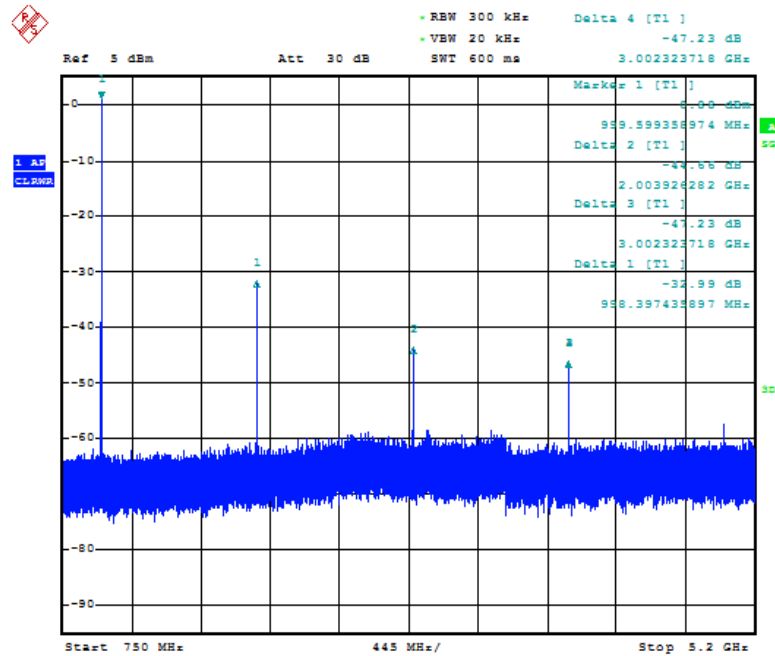
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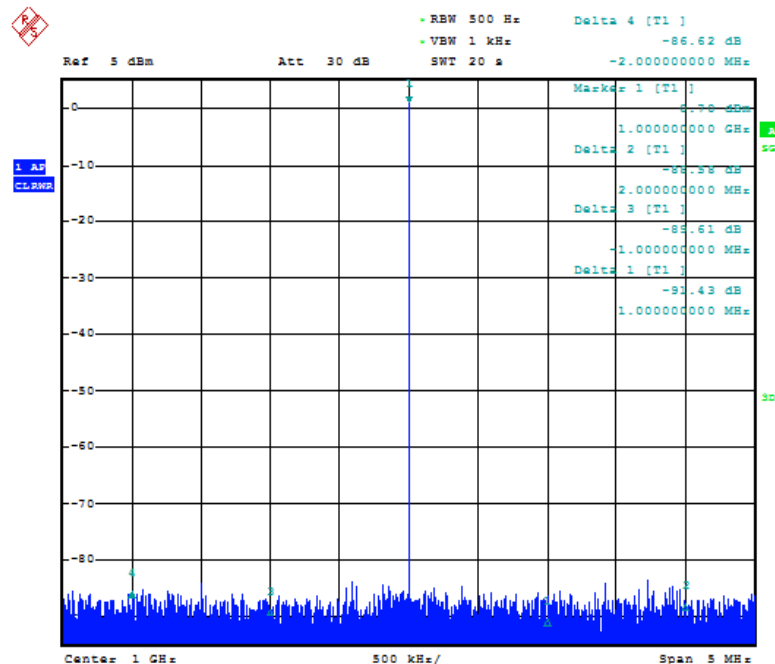
@ +25 °C

PERFORMANCE PLOTS

HARMONIC SUPPRESSION



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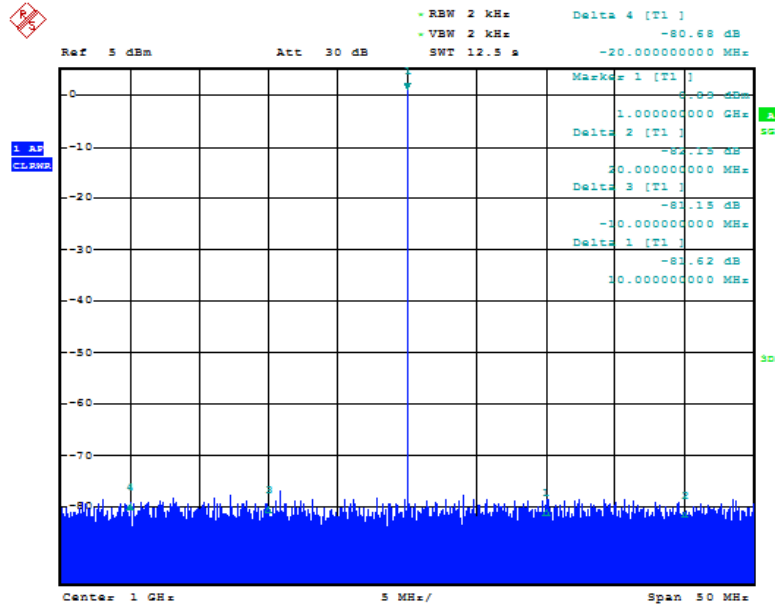
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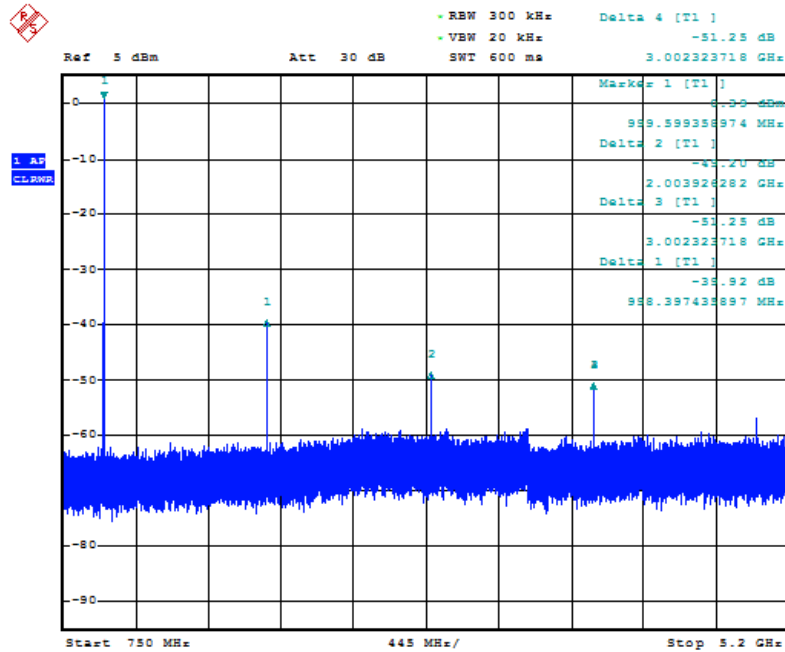
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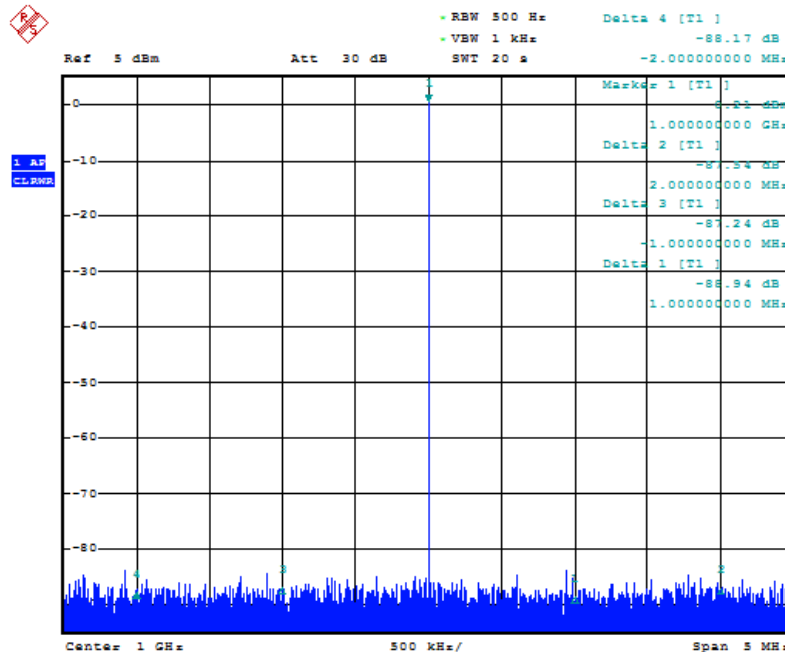
1000 MHz

HARMONIC SUPPRESSION

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PERFORMANCE PLOTS

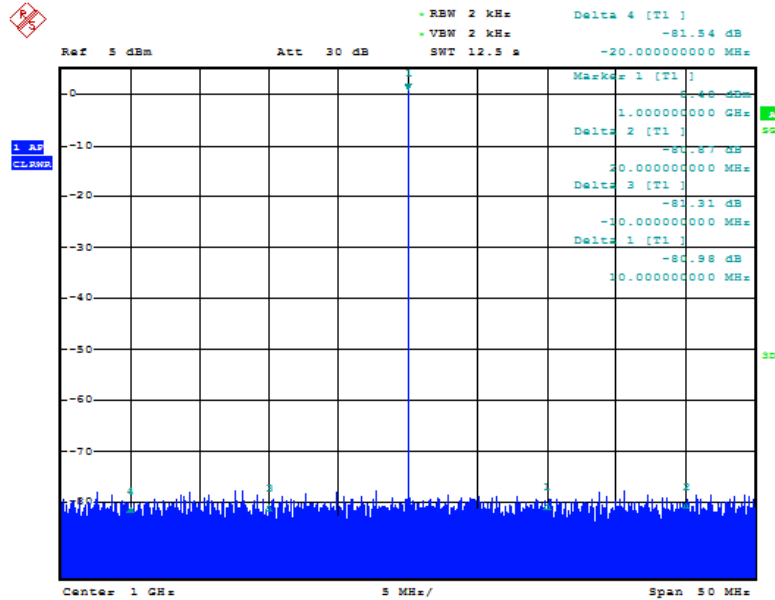
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